

業績書（教育職員免許法施行規則第 22 条の 6 号関係）

氏 名	望月誠二	学 位	博士（工学）
担当授業科目	情報と職業		

1 経歴，学会及び社会における活動等

経歴	
(株) 日立製作所 情報映像メディア事業部 システム LSI 開発センター	平成 7 年 4 月～平成 15 年 3 月
(株) ルネサステクノロジ	平成 15 年 4 月～平成 22 年 3 月
(株) ルネサスエレクトロニクス 車載 SoC 開発統括部 車載ソフトウェア開発統括部	平成 22 年 4 月～令和 4 年 12 月
大阪産業大学 工学部 電気電子情報工学科 教授	令和 5 年 4 月～現在に至る

2 著 書

著 書 名	単著・共著の別	発 行 所 名	刊行年月日	備 考
なし				

3 学術論文等

学 術 論 文 等 の 名 称	単独・共同	発 表 雑 誌 等 名	発行年月日	備 考
A 64mW High Picture Quality H.264/MPEG-4 Video Codec IP for HD Mobile Application in 90nm CMOS	共同	IEEE Journal of Solid-State Circuits	Nov. 2008	
A 256mW 40Mbps Full HD H.264 High-Profile Codec featuring a Dual Macroblock Pipeline Architecture in 65nm CMOS	共同	IEEE Journal of Solid-State Circuits	April 2009	
A Full HD Multi-Standard Video Codec for Mobile Application	共同	IEEE micro	Dec. 2009	

A 342mW Mobile Application Processor With Full-HD Multi Standard Video Codec and Tile-Base Address Translation Circuits	共同	IEEE Journal of Solid-State Circuits	Jan. 2010	
A 197mW 70ms-Latency Full-HD 12-Channel Video-Processing SoC in 16nm CMOS for In-Vehicle Information Systems	共同	IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences	Dec. 2017	
A 12-nm Autonomous Driving Processor With 60.4 TOPS, 13.8 TOPS/W CNN Executed by Task-Separated ASIL D Control	共同	IEEE Journal of Solid-State Circuits	Jan. 2022	

4 学会発表等

発表課題の名称	単独・共同の別	発表学会等の名称	発表年月日	備考
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A Low Power and High Picture Quality H.264/MPEG-4 Video Codec IP for HD Mobile Applications	共同	IEEE Asian Solid-State Circuits Conference	Nov. 2007	
A 256mW Full-HD H.264 High-Profile CODEC Featuring Dual Macroblock-Pipeline Architecture in 65nm CMOS	共同	IEEE Symposium on VLSI Circuits	June 2008	
Low-complexity Intra-prediction for H.264/AVC Using Pseudo Local Decoded Image	共同	IEEE International Conference on Consumer Electronics	Jan. 2009	
Development of Full-HD Multi-standard Video CODEC IP Based on Heterogeneous Multiprocessor Architecture	共同	IEEE Asia and South Pacific Design Automation Conference	Jan. 2009	
A 342mW Mobile Application Processor with Full-HD Multi-Standard Video Codec	共同	IEEE International Solid-State Circuits Conference	Feb. 2009	
An 80 mW Dual Video-Codec SoC for Seamless Playback of Digital Terrestrial Television and Mobile Broadcasting Services	共同	IEEE International Symposium on Consumer Electronics	June 2010	
Extended Variable-length Mode Coding for Enhancement of H.264/AVC	共同	IEEE International Conference on Consumer Electronics	Jan. 2011	

A 768 Megapixels/sec Inverse Transform With Hybrid Architecture For Multi-Standard Decoder	共同	IEEE International Conference on ASIC	Oct. 2011	
Intra Texture Prediction Based on Repetitive Pixel Replenishment	共同	IEEE International Conference on Image Processing	Oct. 2012	
A 0.51ms Low-latency & Variant Bitrate H.264 Video Decoder for Surround View Monitoring and Car Infotainment	共同	IEICE International Conference on Integrated Circuits, Design, and Verification	Aug. 2015	
A 197mW 70ms-Latency Full-HD 12-Channel Video-Processing SoC for Car Information Systems	共同	IEEE International Solid-State Circuits Conference	Feb. 2016	
71% reducing the memory bandwidth requirement for a multi-standard video codec by lossless compression of video using a combination of 2D-DPCM and Variable Length Coding	共同	IEEE International Conference on IC Design and Technology	June 2016	
16.8 GB/s LPDDR4-3200 @32-bit Memory Access Bandwidth	共同	IEICE International Conference on Integrated Circuits, Design, and Verification	Oct. 2017	
Ultra-low-latency Video Coding Method for Autonomous Vehicles and Virtual Reality Devices	共同	IEEE International Conference on Internet of Things and Intelligence System	Nov. 2018	

Design and Implementation of Ultra-Low-Latency Video Encoder Using High-Level Synthesis	共同	IEEE International Symposium on Intelligent Signal Processing and Communication Systems	Dec. 2019	
A 12nm Autonomous-Driving Processor with 60.4TOPS, 13.8TOPS/W CNN Executed by Task-Separated ASIL D Control	共同	IEEE International Solid-State Circuits Conference	Feb. 2021	

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