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Summary of Crystalline Defects Control in Silicon

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Abstract

This report summarizes major silicon (Si) crystal challenges to control process-induced microdefects, oxidation-induced-staking fault, oxygen precipitation, plastic deformation and/or warpage (thermally-induced and/or gravitational-induced dislocation), getttering, crystal originated particles in Si, and to review controlled point-defects in the Si crystal in parallel with the evolution of Si microelectronics from integrated circuit through the ultra-large-scale-integration era from 1970s through 2010s. Furthermore, recent development related to point-defect dilemma during the Si crystal growth from 1980s through 2010s will also be reviewed.

Key words: dislocation-free Si single crystal, integrated circuit, ultra-large-scale-integration, stacking fault, dislocation, plastic deformation, warpage, oxygen precipitation, gettering, vacancy, interstitial, metal contaminants

1. Introduction

1.1 Objective and scope

A dislocation is an essential crystalline defect for an understanding of many of the physical and mechanical properties of crystalline solids.[1-7] Electronic-grade silicon (Si), occurring naturally in the form of silica and silicate, is the most significant semiconductor for the electronics industry. In this report, we focused on crystalline defects in dislocation-free Si single crystals aiming at the perfect basis (wafer) for Si electronic devices.[8-13]

Historically, a transistor was invented in 1948 (a transistor of rudiment was fabricated in germanium (Ge) substrate). It was the dawn of a new era into an incredible development of the current Si electronic devices. Then, in 1960, integrated circuit (IC) was exploited on the basis of the epoch making concept in which transistors, capacitances and resistors were concurrently embedded in the Ge substrate. Nowadays, the remarkable advance into ultra-large-scale-integration (ULSI) device leads to the innovative computer and communication age.[8-13] Since 1965, all kinds of IC and/or ULSI devices have been manufactured in Si wafer in which a Si crystal ingot has been sliced, lapped, etched and mechano-chemical mirror-polished on one side and cleaned (see the Si ingot and wafers in Fig. 1) before the electronic devices are fabricated in the surface area of the Si wafer.

At the moment in 2016, a miniaturization of ULSI device is still proceeding, a half pitch of the device which is a criterion of the miniaturization advances from 16 to 11 nm. According to SEMI report, the limit of the miniaturization may be 5 nm in the future. Concurrently, a wafer enlargement is groping toward from 300 to 450 mm in diameter aiming at manufacturing cost effective devices.

In parallel with the evolution of the Si IC and/or ULSI devices, Si crystal technology has remarkably been added value to those devices for the last 60 years. In 1958, Dash[14,15] showed the possibility of dislocation-free Si crystal growth by necking method which has been developed into float-zoning (FZ)[16] and Czochralski (CZ)[17,18] growth methods. Many research activities have been aimed at growing dislocation-free Si crystals.

Upon remelting process during Si crystal growth, point defect clusters are introduced into crystals.[19-25] In 1970s, swirl defects (point defect clusters) were postulated to be generic term referring to a class of defect structure in Si dislocation-free crystals in which point defect complexes were condensed.[19-25] Shallow pits of the defects were found to be distributed in a swirl-like pattern by etching method,[19,20] reflecting the combined effects of melt convection, rotation of the crystal and temperature fluctuations at the crystal-melt interface during crystal growth as shown in Fig.2.[20] These are summarized in connection with microdefects (grown-in defects) later in detail (see section 3.1 below).

In the early 1970s, the commercial introduction of dislocation-free FZ and CZ Si single crystals began. Since then, most of Si electronic devices have been fabricated on dislocation-free CZ Si wafers in comparison with the FZ

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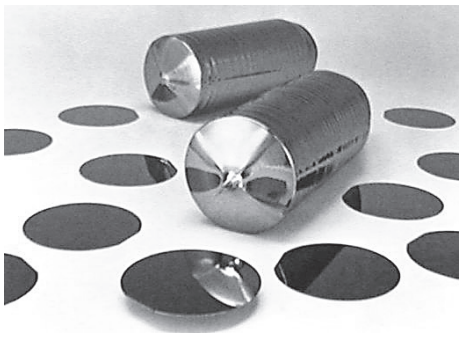

Fig. 1 . A view of Si single crystal ingot and mirror-polished wafers.

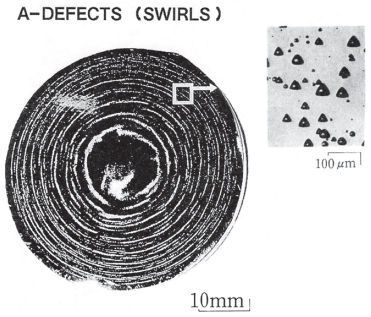

Fig. 2 . Swirl distribution and shallow pits in 35-mm-diameter dislocation-free FZ single crystal [Copyright (1966) The Japan Society of Applied Physics].[20)]

crystal. In view of the importance of the oxygen content for intrinsic gettering (IG)[26)] (see gettering section 1.5, 2.5, 3.5 below) and considering the effect of uncontrolled oxygen content in plastically deforming and warping the wafer, the comprehension of oxygen behavior in Si during processes became very crucial. Detailed investigations will be implemented later.

In general, CZ Si wafers are mechanically stronger than FZ wafers during heat treatments at high temperatures. This is because the former of oxygen content is much higher (approximately three orders magnitude high) than the latter, thereby, even if slip dislocations are once generated, induced dislocations are promptly pinned by oxygen (locking effect: what is called Cottrell effect).[1,27-29)] Hence, the further multiplication of dislocations was prohibited in CZ Si single crystal. Thus, CZ Si wafers were lesser susceptible to the occurrence of slip dislocations or warpage due to thermal stresses than FZ Si wafers. However, in CZ Si wafers for device processing, the crucial problem of thermally-induced dislocations[29-33)] became remarkable as wafer size was enlarged from 2 to 3 inch in 1970s. Those dislocations were induced by thermal stress in regularly-spaced circular Si wafers.[30-34)] The typical induced-dislocation etch pattern in (111) wafer along the $<110>$ slip direction is illustrated in Fig. 3.[9)] Namely, harmful effects by dislocations in electrical performance became remarkable in 1970s (era of 3 inch wafer size). The relationship between enlargement of Si wafer and growing thermal stress will be discussed later in detail.

In 1990s, concurrently, regarding large diameter wafer (200 mm [8 inch] diameter wafer), the gravitational stress caused the introduction of slip dislocations at high temperature treatments.[35-37)] This problem was solved by the improvement of wafer supporting jig. This will be also described later in detail (see section 3.4 below).

In dislocation-free CZ Si single crystals, point defects including vacancy, interstitial and impurities such as oxygen are incorporated into crystals during growth around at melting temperature. In the course of crystal growth and cooling processes, various secondary defects are created in the form of swirl,[19-24)] nuclei and/or oxygen precipitates[38-43)] and crystal originated particles (COP) (see section 1.6 below).[44)] These microdefects have critically affected crucial failure to electrical performance of miniaturized Si devices.

In 1970s, the occurrence of oxidation-induced stacking fault (OSF) also became a crucial problem that researchers should get over it to improve electrical characteristics in Si devices.

Oxygen with high content (the oxygen content was as high as $\sim 2.0\times10^{18}$ atoms/cm^3) in CZ Si wafers, although electrically neutral, agglomerates as oxygen precipitates SiO_2 during high temperature heat treatments. The oxygen precipitates in the bulk aggravated the reduction of mechanical strength of Si wafer, as it were, precipitation softening, accelerating warpage of the wafers due to thermal stress.[45-49)] On the other hand, oxygen precipitates SiO_2 give rise to punched-out dislocations and stacking faults to relax the stresses because lattice parameter of SiO_2 is approximately two times larger than that of Si lattice. Then, unwanted impurities were absorbed in stress field of the punched-out dislocations and stacking faults (scavenging effect) and those impurities were made inactive in electrically active p-n junction area in

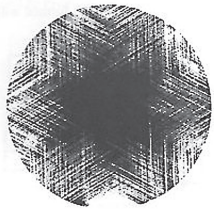

Fig. 3 . A (111)-oriented Si slice in which the severe slip has been delineated by etching to show the emergence of dislocations. The lines lie along the intersection of other (111) slip planes with the viewing surface.

devices.

The latter phenomenon has been called an intrinsic gettering（IG）(see gettering section 1.5 below)[26] compared with extrinsic gettering（EG）such as backside damage, poly-Si film and implanted layer in Si wafer（see gettering section 1.5 below）. Until recently, many investigations have been performed and substantial benefits have been confirmed in devices for the past several decades.

In this report, we focus on controlling crystalline defects in CZ Si wafers including growth-induced microdefects caused by point defects（vacancy and interstitial）and oxygen, and also device process-induced defects［oxygen precipitation, OSF, thermally-induced dislocations, gravitational-induced dislocations, IG and crystal originated particles（COP）defects］.

1.2 Crystal growth-induced microdefects

In ULSI device era, each device is necessary to be fabricated in sophisticated Si wafers. The wafers are sliced from dislocation-free CZ single crystals, lapped, etched and mechano-chemically mirror-polished on one side and then finally cleaned. Therefore, to manufacture a commercially high quality CZ Si crystals has been a crucial assignment with an aim of the evolution into the state-of-the-art Si electronic devices since 1970s..

In as-grown state of dislocation-free crystals, the Si wafer includes point defects such as vacancy, self-interstitial and impurities（especially oxygen atom）. In 1970s, swirl defects were postulated to be generic term referring to a class of defect structure in dislocation-free crystals in which point defect complexes were found to be developed as a result of the condensation of intrinsic point defects.[19-25,50] Kolbesen, de Kock and their colleagues[24,25] showed that swirl defects in FZ Si（referred to as *A* defects）were agglomeration of interstitial atoms, rather than vacancy, dislocation loops and by their detailed models, and they showed that the *A* and *B* defects were significantly different. The *B* defects were suggested to originate from droplet-like agglomerates of interstitials.

Over and above the point-defect dilemma, an increased understanding of the incorporation of point defects into the solidifying Si crystal was also being obtained.[50] The crystal growth, sectioned along the direction of crystal growth, was observed by Abe[50] to generally exhibit a spatial demarcation between vacancy-rich and interstitial-rich regions, depending on the crystal growth parameters.

In 1982, Voronkov[51] suggested that the dominant type of intrinsic point defects were vacancy and/or self-interstitial incorporated into the Si crystal during CZ growth and they depended on the ratio V/G , where V is the growth rate and G is the near-interface axial temperature gradient. Voronkov and Falster[51,52] argued the conditions of incorporation of vacancies and/or interstitials into Si crystals in terms of the ratio V and G. In the early 80's, Voronkov[51] put forth a model that vacancy-rich crystal is grown for larger V/G, while interstitial-rich crystal is grown for smaller V/G. A defect-free crystal was obtained only when the V/G lies in between these two regions. Since then, Voronkov model[51] has been attaining the standard position as the model of defect growth of Si over 30 years. In this model, V and G are regarded as two independent parameters.

On the other hand, in Abe's model,[50] it is assumed that only vacancies are introduced at the melt/solid interface by thermal gradient. In Voronkov's model,[51] both vacancies and self-interstitials are incorporated with their thermal equilibrium concentration. Tuning the crystal-growth parameters was subsequently shown by Voronkov[51] and later, in conjunction with Falster,[52] to result in either vacancy-rich or interstitial-rich material. Interstitial-rich material was found to result in an improvement in gate-oxide-integrity（GOI）in ULSI devices. Otherwise, when V was moderately high, vacancy became rich and coalesced as voids（see section 1.6 and 3.1 below）. The void region of a crystal was surrounded by a narrow marginal band of particles, and in 1989, this band was identified to be the formation of the ring-shaped stacking fault（R-SF）[53] that was found after annealing at high temperature（see section 3.1, 3.3 regarding R-SF below）.

Nevertheless, until 2011, Abe and co-workers[50,54-56] have noted the greater importance of the thermal gradient, per se, at the crystal-melt interface in controlling the formation of point defects. They developed their theory based on that the growth rate of Si crystals depends on the temperature gradient, thereby causing thermal stresses to introduce point defects. In 2016, Abe and co-workers[57,58] claim that at the melt/solid interface only vacancies are introduced into the growing crystal while interstitials are generated in the already grown crystal when thermal stress increases sufficiently e.g. due to the larger thermal gradient when pulling slowly in contrast to Voronkov model.[51,52] Vanhellemont[59] already estimated the effects of thermal stress on point defects on the basis of the calculation of the first principle.[60-63]

Nowadays in 2016, Vanhellemont et al.[64], commented the former Abe and co-worker's idea[57,58] against Voronkov's model[51] and concluded that the explanation of their observations was partly based on assumptions that were not correct and might therefore be misleading. However, the generation of point defects and the formation of secondary microdefects during CZ Si crystal growth is still controversial. This will be discussed in section 3.1 below.

1.3 Introduction of slip dislocations due to thermal stresses in CZ Si wafers during device processing

During Si electronic device processing in 1970-1980s, when a row of regularly-spaced circular Si wafers is inserted into or pulled out of a furnace maintained at high temperature, a thermal stress was set up in each wafer as a result of the radial variation of the temperature.[30-34] Major reason of the thermal stress was caused by shadowing effects between wafers in a row.[31] If the thermal stress in a (111) plane along the<110>slip direction exceeds the critical shear stress of the wafers, slip dislocations or warpage can be initiated, depending on several factors; the wafer processing temperature and the temperature gradient on the wafers, the type of microdefects due to oxygen precipitation[65] and their amount,[45,66,67] the wafer dimensions (the diameter-thickness ratio), and the direction of initial bowing.[45,66,67] In ULSI processing, oxide precipitates,[68] as well as punched-out dislocations around them,[65,67] act as sites for slip dislocation generation, causing plastic deformation of wafers (warpage).

To reduce the warpage due to thermal stress during device processing has been one of the major problems in larger-diameter CZ Si wafers (4 inch or greater) in order to obtain higher production yields of devices. Minimizing the wafer warpage was shown to be facilitated by reducing the insertion/withdrawal rate from the furnace less than 850 °C, as shown by Shimizu et al.[48,49] The mechanical properties of Si crystals had been investigated in relation to the behavior of oxygen.[27-29,68,69] In CZ Si wafer containing oxygen as high as $\sim 1.0 \times 10^{18}$ atoms/cm^3, induced dislocations are immediately locked by oxygen (locking effect),[29] resulting in the prohibition of further multiplication of dislocations. However, in CZ Si wafers, oxygen atoms in excess of the solubility limit precipitate at the elevated temperatures of around 1000 °C commonly employed in ULSI processing, resulting in secondary and/or third lattice defects which give rise to both beneficial and detrimental effects in ULSI devices. Microdefects induced by oxygen precipitation treatment, if properly controlled in the bulk of the wafers far from the surface, act as capturing sites for harmful impurities on surface region, what is called, IG.[26] On the other hand, such microdefects (oxide precipitates, punched-out dislocations and stacking faults) degrade p-n junction characteristics if they penetrate into the active device area, and also serve as sources for slip dislocation generation and multiplication. This phenomenon is called crystal softening effect.[29]

Oxygen precipitation in CZ Si at high temperature annealing is strongly influenced by the oxygen concentration, carbon concentration,[70,71] and thermal history (cooling conditions of crystal ingot after growth) and subsequent oxygen stabilization heat-treatment (annihilation of oxygen donors formed at around 450 °C).[72] This will be discussed in section 1.5 and 3.6 later.

Issues of slip dislocations become crucial as wafers are getting larger because of shadowing effect between wafers or weight, although groped by wafer manufacturing company toward from 300 to 450 mm in diameter in the near future.

1.4 Occurrence and elimination of oxidation-induced stacking faults

Upon oxidation of Si wafers at high temperature (900-1200 °C), stacking faults often occur on Si surface. This stacking fault was firstly observed in 1963 by Thomas[73] and was called oxidation-induced stacking fault (OSF or OISF), degrading electrical performance of Si devices. This was discriminated from the bulk staking fault (B-SF) which is originated in oxygen precipitation in Si bulk. The nucleation and growth mechanism of OSF had been investigated in detail, although, it was postulated to nucleate at scratches, residual damages and/or contaminants at wafer surface and grow during oxidation in which interstitial atoms are collapsed.[74,75] Therefore, from lattice defect point of view, the structure of OSF is an interstitial-type (extrinsic) stacking fault on (111) plane which is surrounded by Frank partial dislocations having Burger's vector of a/3<111>.[2] Following the definition by Frank,[2] the extrinsic stacking fault is surrounded by Frank partial dislocation, where an extra half plane is inserted, as it were, it corresponds to the insertion of interstitial atomic plane. The nucleation sites of OSF were already known at scratches, residual damage, contaminants and swirl defects at the surface of Si wafers.[76-79]

In oxygen precipitation during high temperature treatments, oxide precipitates (SiO_2) emit excess interstitial Si atoms, causing interstitial-type punched-out dislocations and B-SF,[38-43] because of the expansion of SiO_2 in Si

lattice.

In order to avoid harmful effects caused by OSF in 1970-1980s, some annihilation and elimination methods had been developed.[80-87] An annihilation of OSF needs that Frank partial dislocations surrounding OSF absorb vacancy. Then, OSF shrinks under annealing at high temperature in non-oxidized ambient. Shimizu et al.[86,87] reported that OSF shrank by annealing the oxidized wafers in N_2 atmosphere and OSF-free region (denuded zone: DZ) could be formed beneath the SiO_2/Si interface area, where the depth of the free region depended on annealing temperatures and time. They have proposed this process to be "post-oxidation annealing" technique.[87] Concurrently, the addition of HCl and Cl gas into oxidized atmosphere also gave rise to the shrinkage of OSF.[83,84]

In 1989, Hasebe et al.[53] reported for the first time that R-SF occurred in ring-likely shape after high temperature annealing. The R-SF is an interstitial-type stacking fault in the bulk and has the same characteristic of OSF. Thus, R-SF is essentially B-SF related to crystal growth in contrast to OSF on the Si surface, and also originated in not only by oxidation, but also by various heat treatments in non-oxidized environment (see section 3.1, 3.3 above and below).[53,88-90]

1.5 Gettering (Extrinsic gettering, intrinsic gettering)

In Si device manufacturing, cleaned wafers are inevitably exposed to metallic contamination environment during oxidation and various processes. In order to avoid harmful effects due to such contaminations on device performances, an idea of the gettering was born and applied in Si device processes.

In 1960, Goetzberger and Shockley[91] firstly reported instance of gettering in Si wafers, where they utilized a phosphosilicate glass (PSG) thin film on the back surface of the Si wafer to getter unwanted metallic impurities away from the active device regions (p-n junction region in front surface).[91] It was initially believed that the metallic impurities were incorporated within the PSG liquidus due to chemical action with P atoms.[91] Figure 4 illustrates a basic concept of gettering by PSG thin layer at the back side of Si wafer. Thus, the gettering process essentially provides a technique to remove the process-induced metal contaminants from active device regions, resulting in realizing an improved device performance, device yield and reliability in the early stage of Si device development. Furthermore, as is described below, the idea of the gettering was successfully applied to Si device processes in alternative ways approximately for the following 40 years longer (see gettering descriptions below).

Thus, the benefits of the gettering were observed in improving device characteristics of p-n junction; the decrease of oxide leakage current and gate-oxide breakdown and so forth. The successful gettering technique required three steps. These steps were (1) the release of metal impurities from their deleterious location within/near the p-n junction, (2) the transport of the metal impurities to the gettering area, and (3) the capturing metal impurities at the gettering site.

A variety of back-surface external and/or extrinsic gettering (EG) technique were subsequently examined.[92] Those were back side mechanical damage,[93] ion-implant damage,[94,95] polysilicon layer gettering.[96] The mechanical damage procedure, however, was prone to particulate flaking off the back-surface. Back-surface polysilicon gettering was a cleaner procedure and was extensively utilized.

On the other hand, the internal and/or intrinsic gettering (IG)[26] technique essentially uses the effect of stresses caused by oxygen precipitation including punched-out dislocations in the bulk.[38-43] Figure 5 shows a schematic picture of the basic concept of IG in which wafer is formed by the combination of DZ in the surface area and microdefect regions which act as gettering sites in the bulk. The pre-dominant method of gettering became oxygen IG with implantation of a defect-free DZ near the surface and microdefects (oxide precipitates, punched-out dislocation complexes and B-SF) in the bulk. When it comes to successful IG, it is required to understand the mechanism of oxygen incorporation and to realize controlled concentration, and also to keep spatial homogeneity of oxygen during CZ crystal growth. This will be discussed later in detail.

Historically, the IG phenomenon was first reported in 1976, what is called, as in-situ gettering.[97] In 1977,[26] this phenomenon has been named as "intrinsic gettering". It was a crack of dawn of IG era and also the beginning of the research and development of IG[98-103] which contributed to the improvement of Si device characteristics. The key elements of IG are to create bulk defects which are necessary to capture deleterious impurities from device active regions and, at the same time, to form DZ beneath the surface. The DZ corresponded to stacking fault-free region which Shimizu et al.[87] insisted in 1978, however unfortunately, they put a high premium on eliminating OSFs, thereby they missed to identify the crucial effects of oxide precipitates in the bulk and absorption of harmful surface

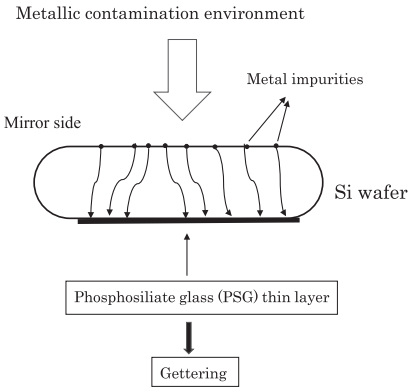

Fig. 4. A basic concept of gettering by PSG thin layer at the back side of Si wafer proposed by Goetzberger and Shockley[91] in 1960. Harmful impurities in wafers were absorbed to PSG thin film because of chemical action with P atoms. This gettering process was successful to have realized an improved device performance, device yield and reliability in the early stage of Si device development.

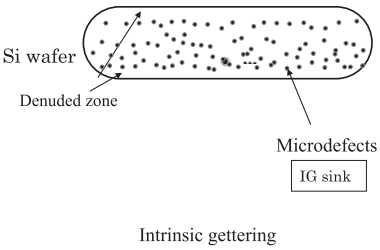

Fig. 5. A schematic of cross-sectional view of intrinsic gettering in the wafer

impurities from device active area into stress field of microdefects. On the contrary, researchers (school of thought of IG) focusing on bulk microdefects contributed to improve device performance by eliminating metal contaminants from device active region. Therefore, the researches and applications of IG into device processes continued for the next 20 years. Nowadays in 2016, impurities on wafer surface becomes more crucial in state-of-the-art ULSI devices in which the half pitch are proceeding from 16 to 11 nm.

1.6 Crystal originated particle (COP) caused by agglomeration of vacancy during crystal growth

In Fig. 6, it is illustrated that a schematic drawing of incorporation of vacancy and/or interstitial into Si crystal ingot during crystal growth. Then, frozen vacancies coalesce into the octahedral void in the course of cooling of the ingot in the CZ growth furnace. According to many researchers, COPs on Si wafer surfaces have been identified as truncated octahedral voids.[104-106] Namely, during crystal growth, vacancies are incorporated liquid/solid interface as shown in Fig. 6, and congregate as the octahedral void surrounded by (111) plane in the course of cooling in CZ growth furnace. To be exact, vacancy rich and/or interstitial rich region in Si crystal ingot were determined by the two parameters of V and G, where V is the growth rate and G is the near-interface axial temperature gradient (Voroncov model).[51] The octahedral voids of the origin of COP are formed when V is rather high. This will be discussed in section 3.1.

CZ crystal ingots are usually sliced to an appropriate thickness, lapped, etched and then mirror polished on one side. Finally, those wafers are treated by a standard clean 1 (SC-1; RCA alkaline rinse) for Si devices. As shown below, COP defects were originally discovered on Si wafer surface in the course of the SC-1 cleaning process.[44] Figure 7 illustrates various type of COPs on the Si (100) wafer in which octahedral voids in the bulk are truncated by the (100) surface. The COP defects revealed on the surface were covered by oxide film (~5 nm), probably because the inside of (111) surface of octahedral void was oxidized during crystal growth.

Historically, the discovery of COP defect dates back to in 1990. Ryuta et al.[44] firstly reported crystal-originated singularities on Si wafer surface by a particle counter after the SC-1 solution.[107] The observed singularities were etch pits (0.1-0.2 μm) and they increased by repeating SC-1 cleaning.[44,108] Based on the further researches, as shown before, the singularities on the Si surface were

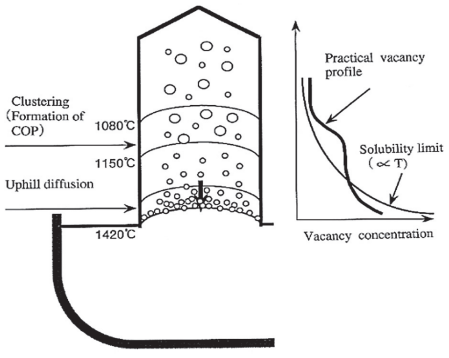

Fig. 6. A schematic drawing of incorporation of vacancies into Si crystal ingot and of coalescence of the octahedral void (LSTD) in the course of cooling of the ingot in the CZ growth furnace.

identified to be COP defects and the origin of COP defect was proved to be a part of an octahedral void which vacancy agglomerated in the Si bulk crystal, where vacancy was incorporated into liquid/solid interface during crystal growth. This was clarified by Voroncov' criteria[51] reported before. Voronkov[51] put forth a model that vacancy-rich crystal is grown for larger V/G, while interstitial-rich crystal is grown for smaller V/G. The COP defects were formed in larger growth rate of crystal region (large V/G), which is vacancy-rich region.

In 1996, Gonzalez et al.[109] firstly reported harmful effects of COP defects on device characteristics. Concurrently, the COP defects were found to be the same origin already characterized as flow pattern defect (FPD),[110] Secco etch-pit defect (SEPD)[111] and laser scattering tomography defect (LSTD).[112,113] These results were investigated by many researchers from 1993 to 1996.[104-106] Kato et al.[106] reported clearly the relationship between LSTD and COP by transmission electron microscopy observation in CZ Si crystal. This is schematically shown in Fig. 8.

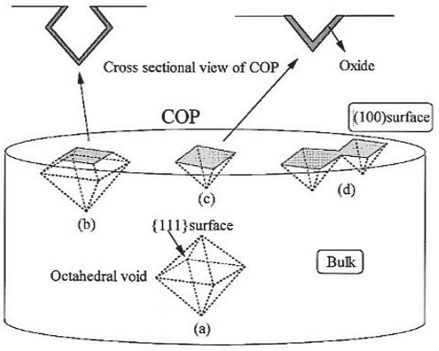

Fig. 7. Schematic diagram of COP defects, (a) shows an octahedral void in Si bulk surrounded by (111) plane (LSTD); (b), (c) and (d) illustrate COPs truncated by (100) surface, (b) is overhang shape and (d) is twin-type.

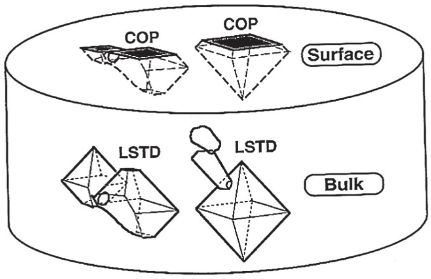

Fig. 8. Schematic view of the relationship between LSTDs and COP defects [Copyright (1996) The Japan Society of Applied Physics].[105]

1.7 Cleaning technology of Si wafers (heavy metal control)

As device dimensions continue to shrink in ULSI circuits, there is a growing need for better control of heavy metal contamination such as Fe, Cu, Ni and Al in both Si wafers and device processings. The economy of device is a direct function of the yield and performance of process steps in device processings. Competitive edge in manufacturing ULSI must process wafers correctly, with perfect consistency and repeatability in Si bulk characteristics such as oxygen concentration, what is called, IG.[26] The progress in chemical analysis is driven by the demands of technology improvements and is getting closely connected with both the Si bulk and device processings, facilitating monitoring on the basis of trace-analysis methods. To monitor impurity level in processings, the trace-analysis methods must be highly selective and of high precision, with high throughput.

2. Experimental procedures

2.1 Shrinkage and annihilation of OSF by post-oxidation annealing method

Dislocation-free CZ Si crystal wafers of (111) and (100) orientations were used. The resistivity was 5-8 ohm-cm (phosphorus doped). The crystals had 1×10^{18} atoms/cm^3 of oxygen and 2×10^{16} atoms/cm^3 of carbon, as determined by infrared absorption measurement. The wafers had been sliced, lapped, and chemically etched in order to remove any damage and then one side of the wafer was chemically-mechanically polished. These wafers were found to generate spiral-shaped patterns, referred to as "swirl", when subjected to the oxidation and Sirtl-etch examination.[114] OSFs were generated after thermal oxidation along swirl pattern. Swirl patterns were clearly visible in the periphery of wafers and hazy in the center of wafers. The OSF densities were $2\text{-}3 \times 10^5$/cm^2 on swirl and $1\text{-}9 \times 10^4$/cm^2 off swirl patterns.

At the first step, oxidation was carried out to introduce OSFs in Si wafers. The wafers were oxidized at 1100 °C in wet oxygen atmosphere saturated with water vapor at 96 °C. To obtain OSFs with several micro-meters in length, the triple sequential oxidation process was applied. These oxidized wafers with oxide films were separated into several pieces and then these specimens were subjected to annealing in nitrogen atmosphere for various times at temperatures between 1050 °C and 1250 °C. In order to measure the shrinkage rate of OSFs and observe the in-depth

distribution of stacking faults in crystals (distribution of B-SFs), the specimens of the later experiments were angle-lapped at an angle of 5.80 ° and etched in Sirtl solution,[114] and then examined with an optical microscope.

2.2 Characterization of ring-shaped stacking fault (R-SF)

X-ray topography was employed to verify the overall distribution of crystal defects of the heat-treated wafers. For the measurement, (220) reflection with Mo K α radiation was used. Thermally induced defects in the R-SF[53] region, i.e., stacking faults, oxide precipitates and accompanying punched-out dislocation loops, were examined by means of the transmission electron microscope (TEM). The electron beam energy was 200 keV in the TEM.

As another characterization technique, a scanning photon microscope (SPM) developed by Munakata et al.[115-117] was employed to evaluate R-SF[53] in parallel with X-ray topography. The SPM method based on the theory of an alternating current surface photovoltage (AC SPV)[116,117] can visually evaluate charged states, chemical contaminants, surface imperfections and bulk defects. Upon evaluating bulk microdefects, a probing photon beam (PB) (near infrared) with wavelength of 896 and 1076 nm was used. The PB was emitted from a specially arranged cathode ray tube and was chopped at 2 kHz. The PB with 0.4 mm diameter was projected onto the wafer surface and its incident PB power was 0.39 mW. Penetration depths into wafers of the infrared PB were 33 and 769 mm, corresponding to the peak wavelengths. Thus, the SPM can analyze crystal defects in wafer bulk.

2.3 Slip dislocation and warpage experiments due to thermal stress

Dislocation-free, phosphorus-doped Si single crystals with a resistivity of 8-12 Ω·cm and 100 mm in diameter were grown in the <100> orientation by the CZ pulling method. Regarding warpage experiments using 100 mm diameter wafer, the grown six ingots were subjected to oxygen stabilization heat-treatment (annihilation of oxygen donors formed around 450 °C) at 650 °C for 3 h in a nitrogen ambient. The sliced wafers were lapped, chemically etched in order to remove any damage and then one side of the wafer was chemically-mechanically polished. Special attention was taken in slicing wafers from the ingots, because the oxygen concentration in CZ Si is a function of the axial growth direction. The six ingots named from A to F were separated into seven portions at 50 mm intervals, and wafers were sliced from each portion for the evaluation of (a) oxygen concentration, (b) the microdefect density, (c) warpage experiments and (d) complementary metal-oxide-semiconductor (CMOS) device processing, as shown in Fig. 9.[48] The wafers are denoted by a letter showing the ingot from which they are taken, and a number showing their position in the ingot, starting at the seed-end and increasing in the growth direction. Thus wafer A-1 was taken from the seed-end of ingot A and A-7 was taken from the tail end of ingot A..

The concentration of interstitially dissolved oxygen atoms ([Oi]) was measured by Fourier transform infrared spectroscopy (FT-IR; Digilab QS 300) in the 2.0 mm-thick specimens with mirror surfaces on both sides. The [Oi] was calculated from the absorption coefficient α at 1107 cm^{-1} according to the following equation:

$$[O_i] = 3.1 \times 10^{17} \times \alpha \quad (\text{atoms/cm}^3). \tag{1}$$

In warpage experiments, the sample wafers were set in a Si boat with 5 mm spacing between the wafers, and seven dummy wafers were set on each end of the batch of experimental wafers. The wafers on the boat were brought into and out of the hot zone of the furnace at a rate of 20 cm/min three times (warpage experiment-I), and were then thermally stressed once again at a rate of 35 cm/min in the same manner (warpage experiment-II).[48] After the warpage experiments (I-II), the bow of wafers were measured. At the same time, the microdefect density of the wafers cut from the neighborhood position was measured by counting the etch pits delineated by Wright etchant[118] on (001) surfaces which polished to a depth of about 40 μm by mechano-chemical polishing. Hence, the bow of wafers was plotted as functions of microdefect density. Here, the microdefect density included oxygen precipitates, punched out dislocations and stacking faults.

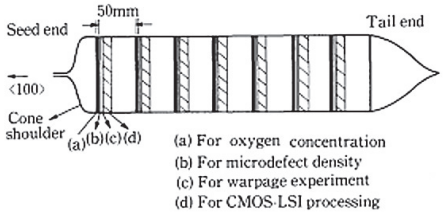

Fig. 9. Pictures illustrating CZ-grown Si crystal ingot separated into several portions with intervals of 50 mm in growth direction. Three kinds of specimen were prepared for each portion of the ingot for the following purposes: (a) measurement of the interstitial oxygen concentration, (b) evaluation of the microdefect density, (c) examination of the warping behavior, (d) CMOS-LSI processing [Copyright (1985) The Japan Society of Applied Physics].[48]

Concurrently, wafers were processed in CMOS device and the bow vs microdefect density relationship was obtained.

Then, warpage experiments depending on oxygen concentration were also performed and the bow vs oxygen concentration was obtained.[49)]

2.4 Thermal stresses calculated by mathematical simulation

In next step, the calculation without experiments was targeted to estimate the onset of slip dislocations due to thermal stresses caused by the radial temperature variation in circular Si wafers. Historically, Hu[119)] was the first researcher to have reported to calculate radial temperature gradient in circular Si wafers, where a row of equally spaced Si wafers were assumed to be set.

Then, Matsuba et al.[120)] developed the thermoelastic wafer model with which to calculate thermal stresses by means of the finite element method (FEM) under plane conditions. Their key elements for obtaining the onset of slip dislocations are based on Hu's[119)] mathematical model. In an attempt to forecast dislocation multiplication due to thermal stresses, the critical stress curves were obtained experimentally as a border of the initiation of slip dislocation against a function of microdefect density on the basis of the mechanical yield stress of Si single crystal suggested by Alexander and Haasen.[121)] In comparison with the estimated mechanical yield stresses of wafers and calculated thermal stresses, Matsuba et al.[120)] proposed the prediction method to initiate plastic deformation of wafers (onset of slip dislocations).

Based on Matsuba et al.[120)] thermoelastic wafer model, Shimizu and Aoshima[122)] described the method to calculate the thermal stresses. In Hu's mathematical model,[119)] the thickness of the wafer was assumed to be sufficiently small so that the temperature could be regarded as uniform across the thickness. The thermal stresses induced by the radial temperature distribution were calculated in polar coordinates in the following:

$$\sigma_{rr}(r) = \alpha E\left[{}^{1}\!/_{R^2} \int_0^R T(r) r\mathrm{d}r - {}^{1}\!/_{r^2} \int_0^r T(r) r\mathrm{d}r \right], \tag{2}$$

$$\sigma_{\theta\theta}(r) = \alpha E\left[{}^{1}\!/_{R^2} \int_0^R T(r) r\mathrm{d}r - {}^{1}\!/_{r^2} \int_0^r T(r) r\mathrm{d}r - T(r) \right], \tag{3}$$

$$\sigma_{r\theta}(r) = 0, \tag{4}$$

where R is the radius of the wafer, r the radial distance from the wafer center, $T(r)$ the radial temperature profile of the wafer, α the thermal expansion coefficient, and E Young's modulus. In the calculation of the radial temperature profile $T(r)$, Hu[119)] assumed that the wafers kept in a high temperature furnace were suddenly placed in an ambient at room temperature and he took three terms into consideration: the radiative heat loss of the wafers, the radiative heat interchange between wafers, and the thermal diffusion of the wafers. However, the thermal exchange between the wafers and the furnace tube wall was neglected. On the other hand, Mokuya et al.[120)] analyzed a transient temperature distribution in the wafers in the case that they were pushed in and taken out of the high temperature furnace at a moderate rate as was commonly employed in device fabrication processes.

As mentioned above, Shimizu and Aoshima[122)] were successful to apply their model to predict the occurrence of the thermal warping of the wafers into and out of the wafer batch from the horizontal-type of furnace.

In order to realize cost effectiveness in manufacturing Si devices, wafer enlargement has been carried out depending on the developments of Si devices year by year. Fig. 10 shows the history of wafer enlargement for the usage in Si devices. Thus, thermal stresses due to radial temperature variation have inevitably become large because of shadowing effect[120)] between large wafers, accelerating the occurrence of slip dislocations. Therefore, in 100-125 mm diameter (4-5 inch) wafer era, in order to reduce thermal stresses, a soft landing method, a state-of-the-art technology in those days, was developed and employed on the manufacturing base. The point of this technique was to insert a wafer batch inside

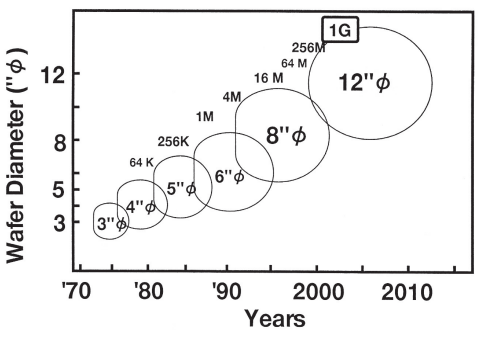

Fig.10. Wafer enlargement vs annual year.

the furnace at lower temperatures in which thermal stress was slightest small, and then heat up furnace into at higher temperatures. This new technique succeeded in almost completely reducing the radial temperature gradient, resulting in the reduction of thermal stresses in large wafers. Since then, this basic idea has been employed in Si device manufacturing processes at high temperatures.

2.5 Slip dislocations and slip bands due to gravitational stress in large diameter wafers

For highly integrated device processing in 1990s, a horizontal-type furnace used for oxidation and diffusion processes was replaced with a vertical-type furnace in which the furnace inside had been designed to use a boat with less heat capacity and to reduce air involvement during wafer insertion and withdrawal. Figure 11 illustrates a prototype of the jig made of SiC that supports wafers in batch-type of a vertical-type of furnace in 200 mm (8 inch) wafer era.[36] In a vertical-type furnace, the circular wafers are set horizontally on a supporting jig, often of the point contact type. At the fulcrum of the jigs, the wafers bow elastically owing to the gravitational stress due to their weight. This stress potentially promotes the nucleation and collective motion of slip dislocations. In this configuration, gravitational stresses in 200 mm-diameter wafers were found to become crucial to potentially initiate slip bands if the gravitational stress exceeds the critical stress for slip dislocations at high temperature processing (especially at around 1200 °C).

We have confirmed that this slip propagation was not caused by thermal stresses, but by gravitational stresses, because the processed wafers were heated up and cooled down slow enough to avoid slip dislocations due to thermal stresses (soft landing technique). Under wafer diameter versus thickness trend designed for ULSI, this gravitational stress increased with wafer size. The gravitational stress promotes slip bands if it surmounts the critical stress of a collective motion of dislocations in Si wafers. Therefore, enlarging the wafer to 300 mm will seriously aggravate the problem of slip band initiation due to gravitational stresses because of the weight of the wafer.

X-ray topography was employed to verify the overall distribution of slip bands and/or dislocations in heat-treated wafers. For the observation, (220) and (422) diffraction with Mo K_α radiation was used. Nuclear plates (Ilford L-4) in place of X-ray films were used to analyze slip dislocation configuration in X-ray topographs.

In order to meet the requirement of 300 mm diameter wafer era, the thermoelastic model by Matsuba et al.[120] was modified to fit the vertical type of furnace by Shimizu et al.[35,37] They took the difference of infrastructure between horizontal and/or vertical-type of furnace into consideration and modified the equations proposed by Matsuba et al.[120] Then, a calculation of gravitational stresses was simulated by FEM under plane stress conditions.[35-37] A wafer was sectioned by both 20 in radial direction and 72 in azimuthal direction, resulting in 1440 elements in all as shown in Fig. 12. Upon the calculation of stress, the wafer was set horizontally in the vertical type of furnace, where the contact point with supporting jig, what is called, the deflection of nodes was fixed zero in cylindrical coordinates and the gravity was assumed to work uniformly across the wafer. Used analytical soft program was a commercially available COSMOS/M (SRAC Co.). The calculated gravitational stresses were converted to resolved shear stresses on slip planes (111) in slip directions $<110>$, which are well defined crystallographic directions in the diamond lattice. X and y direction were defined as shown in Fig. 12. Among the five slip systems, the maximum resolved

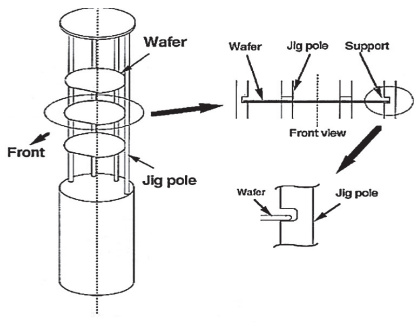

Fig.11. Conventional supporting jig for the beginning of 200 mm-diameter Si wafer to manufacture Si devices in vertical type furnace (Copyright Permission by The Electrochemical Society).[37]

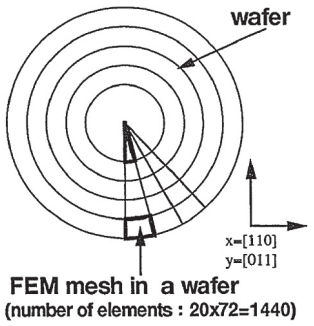

Fig.12. A schematic diagram of meshes in a wafer used finite element calculation of gravitational stresses (Copyright Permission by The Electrochemical Society).[37]

stress was regarded as the gravitational stress required for the present computer simulation as follows:

$$S_1 = \sqrt{2/3}\,|\,\tau_{xy}\,| \tag{5}$$

$$S_2 = \frac{1}{\sqrt{6}}\,|\,\sigma_{xy} + \tau_{xy}\,| \tag{6}$$

$$S_3 = \frac{1}{\sqrt{6}}\,|\,\sigma_{xx} - \tau_{xy}\,| \tag{7}$$

$$S_4 = \frac{1}{\sqrt{6}}\,|\,\sigma_{yy} + \tau_{xy}\,| \tag{8}$$

$$S_5 = \frac{1}{\sqrt{6}}\,|\,\sigma_{yy} - \tau_{xy}\,| \tag{9}.$$

2.6 Procedure of IG

The key elements of IG technique are the following two items, namely, a formation of both DZ and an interior bulk region of high densely microdefects which act as gettering sites (referred to as IG sink) as has been shown in schematics of Fig. 5.

In general, IG heat treatments consisted of the following three steps. The first was the out diffusion of oxygen at high temperature (>1100 °C) in non-oxidized ambient. The purpose of this step was to form DZ in the surface region of the wafer. The second step was to reform grown-in SiO_2 embryos at low temperature (600-750 °C) which had already been shrunken and/or annihilated in the first step. Namely, this step was a formation of nucleation sites of bulk microdefects in the subsequent heat treatments. The third step was the heat treatment (1000-1150 °C) to grow microdefects (SiO_2 precipitates including punched-out dislocations and B-SF) in the bulk which act as gettering sites beneath the DZ. This method was called as denuded zone intrinsic gettering (DZIG).[99]

The function of IG depends on the microdefect density in the bulk in which oxygen concentration plays a key role in IG process. In contrast, the mechanical strength of the Si wafer has been reported to be dependent on the microdefect density.[48] Concurrently, the microdefect density is closely related to oxygen concentration of Si wafers. In high oxygen concentration as high as$\sim 1\text{-}2\times10^{18}$ cm^{-3}, high density of oxide precipitates will cause higher density of microdefects during heat treatments. Therefore, to control reasonable oxygen content in CZ growth is necessary to realize fruitful effects of IG.[123-126]

Anyway, IG was born out of necessity to fabricate sophisticated ULSI devices because slightest small impurities affect the p-n junction characteristics.[127]

2.7 Testing method of defective cells due to COP_S in MOS devices and thin-film epitaxial growth

Device failure due to COP_S was detected as follows. The memory cells in the test element group (TEG), which form the sensing amplifiers, can operate like an actual dynamic random access memory (DRAM). The memory cells were tested by checking the data of the memory cell after a pause refresh time of 100 ms, and were sorted into three defect modes: (i) isolation leakage (word line voltage; 5.0 V, substrate voltage; 0.4 V), (ii) junction leakage (word line voltage; 0.01 V, substrate voltage ; 3.0 V), or (iii) MOS degradation (word line voltage; 0.0 1V, substrate voltage; 0.4 V). The defective oxide and cells caused by the COP_S were observed by using a scanning electron microscope (SEM). The epitaxial layer grown on CZ-Si substrates with a resistivity of about 10 Ω · cm (p-/p- structure) was varied in thickness from 0.01 to 5μm. The growth conditions for p-/p- thin-film epitaxial wafers was as follows. Epitaxial growth was done at 1000 °C by using the decomposition of SiH_4 gas. Dopant impurities, such as boron, were controlled by adding gases such as B_2H_6 during epitaxial growth. The epitaxial layer thickness was determined by using FT-IR to measure the film formed on dummy p+ substrates.

The density of gate oxide defects was evaluated for the test devices. MOS capacitor structures were formed by using one of the following structures: (i) a patterned poly-Si film formed by using chemical vapor deposition

(CVD) in a local oxidation of Si (LOCOS) structure (electrode square: 4.9 mm^2), or (ii) a 4 mm^2 patterned flat Al electrode deposited over an 18.5 nm thick gate oxide film. The density of gate oxide defects (D) was calculated as

$$F = 1 - \exp(-SD) \quad (10)$$

where S is the gate area and F is the cumulative percentage of failure.

2.8 Impurity analysis by the combination of pack extraction method and inductively coupled plasma mass spectroscopy

In Si wafer processes, in general, final cleaning of wafers was subjected to RCA (Radio Corporation of America) alkaline solution (ammonium hydroxide/hydrogen peroxide/water) and/or acid rinse (hydrochloric acid/hydrogen peroxide/water). On the other hand, the wafer cleaning procedure in Si device processings usually uses a combination of RCA solution (alkaline and acid) and an aqueous hydrofluoric acid (HF) solution with a small additional hydrogen peroxide including surfactant. Appreciable amounts of metal impurities (10^9-10^{10} atoms/cm^2) still remain on the cleaned Si wafer surfaces. Hence, the cleaning and its evaluation are major concerns and extensive investigations are being conducted. In the present paper, in order to analyze the small amount of residual impurities, the combination of pack extraction method (PEM) and inductively coupled plasma mass spectroscopy (ICP-MS) was developed. The procedure of PEM will be described in section 3.8.

The ICP-MS is provided with a double-focusing magnetic-sector mass analyzer. The sample solution is introduced into the analyzer at a flow rate of 1.67×10^{-8} m^3/s. Acceleration voltage is 4.7 kV and plasma power is 1.3 kV. The resolution efficiency is 4500 for Fe, 2000 for Al, 3500 for Cu, Cr, Ni, and Zn. Ar is used as a neblizer gas at a flow rate of 0.9 l/min, auxiliary gas is 1.0 l/min, and cooling gas is 13 l/min. The detection limits for Al, Fe, Cr, Cu, Ni, Zn and Co are 2×10^9, 5×10^8, 5×10^8, 5×10^8, 1×10^9, 8×10^8 and 2×10^8 atoms/cm^2.

Extracted solution by the PEM was introduced into ICP-MS and analyzed.

3. Results and discussions

3.1 Crystal growth-induced microdefects

In section 1.2, the history of Si crystal growth-induced microdefects was reviewed. Since Voronkov's model[51] in 1982, huge amount of data have been reported to clarify the point defect incorporation during growth and the mechanism of point defect clustering in subsequent heat treatments has been proposed. On the basis of Voronkov's model[51] and other researchers results,[54-64] we analyzed and summarized point-defect incorporation into the Si crystal ingot and the relationship between pulling rate (growth rate) and temperature gradient at solid-liquid interface during growth, leading to easily understand what kind of crystal could be grown.

Figures 13 (a) and (b) describe the feature of point-defect clustering in the ingot during Si crystal growth [in the left hand figure (a)] and quality merchandise of the wafer depending on pulling rate (growth rate) (V) and temperature gradient at solid-liquid interface (G). In the right hand figure (b), vertical axis is V of Si crystal ingot and horizontal axis is G during crystal growth. If $V/G > \xi$ (ξ : constant) condition holds, vacancy-rich region is formed.[51] In the $V/G >> \xi$ region, voids due to vacancy accumulation and collapse became remarkable, thereby LSTD[112,113] could be formed in the bulk. In the course of wafer manufacturing, the LSTDs are truncated in wafers and then COP defects are revealed on the Si (001) surface (see details section 3.7 below). Moreover, V is a bit smaller region than COP region, R-SF[53] emerges [typical pictures of R-SF is shown in Fig. 14 (see details in section 3.3 below)]. If $V/G < \xi$ condition holds, interstitial-rich region is formed, finally causing interstitial-type dislocation cluster[129] as pointed out by Voronkov et al,[51,52] Machida et al.[130] found that vacancy-rich defect-free region was formed followed by interstitial-rich defect-free region in the exterior of R-SF.[53] On the other hand, Takata et al.[131] realized in Si 400 mm diameter wafers that to shrink vacancy-rich region and to expand interstitial-region made it possible to grow LSTD free crystals, resulting in fabricating COP free wafers. This idea that allows predicting if Si single crystal pulled from a melt will be vacancy rich and/or interstitial rich is the basis for industrial production of grown-in defect-free Si crystals and wafers. Thus, Takata' method[131] will be expected to manufacture Si wafers appropriate for ULSI devices.

Many researchers have done various investigations regarding to point defects on the basis of the model by Voronkov et al.[51,52] for the last 30 years. Thus, they have considered that both vacancy and interstitial atoms in Si crystal are generated from the solid-liquid interface of Si and diffuse toward the lower temperature interior of a

crystal. Moreover, there are differing opinions with respect to whether a decreased crystal pulling rate increases or decreases thermal gradient G in a crystal near growth interface. As described in section 1.4, when the pulling rate is gradually decreased, R-SF,[53] which is confirmed after a heat treatment, is generated as ring shaped band in the periphery of a crystal at a certain pulling rate and then reaches the central portion of the crystal.[57,58]

From 2011 through 2016, Abe et al.[56-58] published beautiful experimental data on intrinsic point defect related to defect distributions in detached growing CZ Si crystals with and without additional thermal anneals. What was new compared to the results published before was that the crystals were pulled with decreasing speed before detaching, resulting in crystals that varied along the axis from initially vacancy-rich to interstitial-rich for the slowest pulling speed before detaching. Based on the analysis of their observations, Abe et al.[56-58] claimed that at the melt/solid interface only vacancies are introduced into the growing crystal while interstitials are generated in the already grown crystal when thermal stress increases sufficiently e.g. due to the larger thermal gradient when pulling slowly. They therefore implicitly rejected the Voronkov model[51,52] that has been the basis for the understanding of grown in defect formation and defect-free Si crystal growth for the last 30 years. Unfortunately, the explanation of their observations was partly based on assumptions that may not be correct and might therefore be misleading.

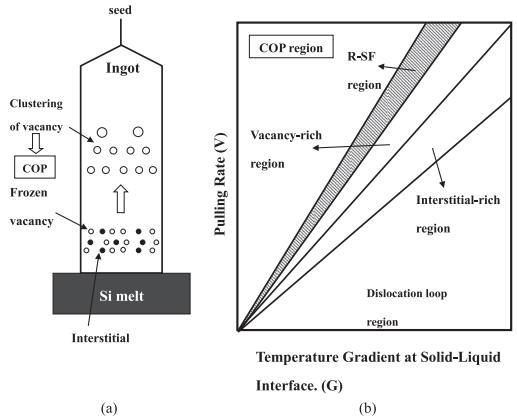

Fig.13. A schematic of vacancies and/or interstitial atoms incorporated into Si crystal ingot during CZ growth and quality merchandise of grown crystals depending on pulling rate (V) and temperature gradient at solid-liquid interface (G). This drawing was analyzed on the basis of Voronkov's model.

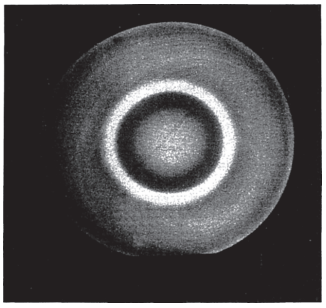

Fig.14. Photovoltage image of R-SF measured with SPM using a near-infrared photon beam [Copyright (1993) The Japan Society of Applied Physics].[90]

In 2016, as described in section 1.2, Vanhellemont et al.[64], commented the former Abe and co-worker's analyses,[56-58] namely, their interpretation of their experimental results. Vanhellemont et al.[64] analyzed and summarized the following three points, contrary to what Abe et al.[56-58] claimed in their three papers: (1) both vacancies and interstitials were introduced in the growing crystal at the melt/solid interface (2) there was no generation of self-interstitials in the grown crystal related to an increase of the thermal gradient, (3) the detached crystal observations could be explained within the framework of the Voronkov's model.[51]

3.2 Shrinkage and annihilation of OSF by post-oxidation annealing method

In this section, we describe the effect of annealing in inert gas (nitrogen: N_2) atmosphere on the shrinkage and elimination of existing OSF and propose this technique, in a sense, be effective in gettering of OSF.[86] Figure 15 shows the variation in the length of OSF as functions of annealing time and temperature. The lengths of OSF decreased linearly with annealing time. It was found that annealing in N_2 atmosphere caused existing OSF to shrink and finally disappear, This fact was verified by the oxidation and Sirtl-etch examination.[114] Furthermore, we obtained the activation energies for the shrinkage process of 4.1 ± 0.3 and 4.9 ± 0.3 eV for (111) and (100) surfaces, respectively, by plotting the shrinkage rates versus the reciprocal absolute temperature on the basis of Arrhenius equation.[86]

Two mechanisms have been proposed for the shrinkage of OSF in silicon,[86] the climb process involving either the absorption of vacancies or emission of interstitials, and the unfaultfng reaction involving the nucleation and motion of Shockley partials,[1,2] Since the activation energy for the shrinkage determined in the present study is 4.1 to 4.9 eV and is consistent with the activation energy for the self-diffusion of silicon 4.78-5.13 eV, it is likely that the shrinkage is governed by the climb process rather than by the unfaulting reaction.

Driving forces necessary for dislocation climbing will be determined by vacancy-concentration gradients between

the fault and its surroundings. According to Sanders and Dobson[80] during oxidation, the vacancy concentration in local equilibrium with the fault is larger than the equilibrium vacancy concentration at the oxidizing surface, and growth of the fault occurs; during annealing in a non-oxidizing atmosphere the vacancy-concentration gradient between fault and surface is reversed and a vacancy flow to the fault gives rise to the shrinkage of the fault.

After the shrinkage of OSF finished at the Si surface, stacking fault-free regions (DZ) were found to be formed underneath SiO_2-Si interface.[86,87] Figure 16 shows the DZ formed beneath the SiO_2-Si interface, when Si wafer was oxidized to generate OSF and/or B-SF and subsequently annealed in N_2 atmosphere at 1150 °C for 10 h. These regions were extended in depth with further annealing. This fact gives direct evidence in favor of the view that the interface acts as a sink for vacancies or interstitials associated with the process of shrinkage.

The benefit of post-oxidation annealing technique was that once a DZ was formed after annealing. no B-SFs were generated in that region, when subjected to subsequent oxidation. This fact would give us a direct evidence that OSF and/or B-SF nuclei were dissolved during the post-oxidation annealing treatment. The clusters of Si self-interstitials and some impurity atoms, particularly oxygen or carbon, were thought to be responsible for the nucleation of B-SF. The above-mentioned heat treatment enabled Si interstitials to migrate to an interface sink at temperatures where the clusters became unstable and eventually dissolved in the matrix. Thus, the post-oxidation annealing had a strong advantage to keep DZ after next heat treatment processes.

The thickness of stacking fault-free regions d followed a power law when $t > t_i$, where t is the annealing time;

$$d = t^n. \tag{10}$$

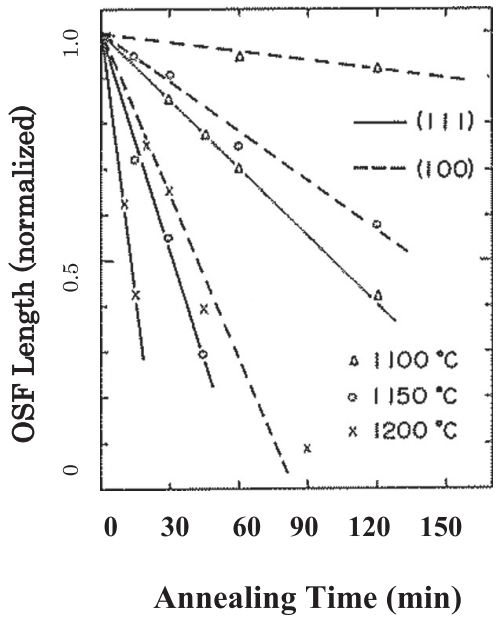

Fig.15. Variation of OSF length with N_2 annealing time.

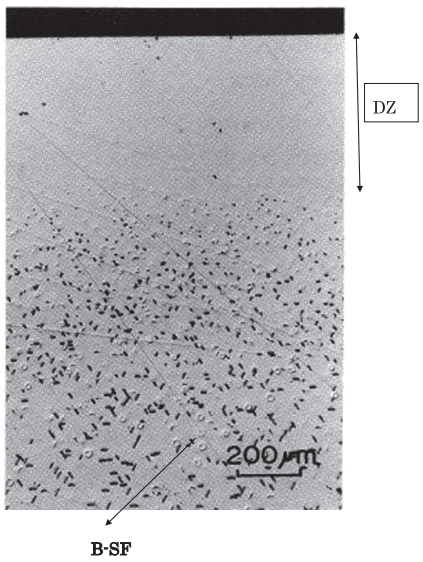

Fig.16. Formation of DZ underneath the SiO_2-Si interface. Cross-sectional view of 6° angle-lapped (111) specimen after the post-oxidation N_2 annealing at 1150 °C for 15 h [Copyright (1978) The Japan Society of Applied Physics].[87]

The exponent n was determined to be 0.63 ± 0.06 from the plot of log d versus log t in Fig. 17.[87]
As reported in the previous paper,[86] OSF shrank linearly in length (n =1) ; the shrinkage rates were nearly equal to the growth rates of the DZ when their thickness was small. However, the growth rates decreased gradually as DZ grew in the bulk crystal because of $n < 1$, giving an indirect evidence that the shrinkage rate of B-SF was apparently small compared with that of OSF (surface). This SF-free regions corresponded to DZ in IG, however, Shimizu et al.[87] focused on the annihilation of OSF, thereby, they did not point out the essence of IG capturing metallic impurities on Si wafer surface which was one of the nucleation sites of OSF. They thought that those impurities were eliminated in the course of annealing of OSF, namely they thought that the stress field of OSF accumulated metallic impurities. However, the basic idea of the post-oxidation annealing was exactly the beginning of gettering technique.

3.3 Characterization of R-SF

As described in section 3.1, many researchers clarified that the nucleation and growth of R-SF[53,89,90] was closely related to crystal growth condition, pulling speed (V) and temperature gradient at solid-liquid interface (G). Furthermore, R-SF was associated with wafer enlargement because R-SF was firstly observed in 100-125 mm diameter wafer.[53]

The wafer samples were heated at 1000 ºC in a wet O_2 ambient for 1 h, followed by another treatment at 1000 ºC in dry O_2 for 15 h.[90] In order to obtain the R-SF distribution, the wafers were for the first step observed by SPM[115-117] as was shown in Fig. 14.[90] Then, the same sample was investigated by X-ray topography which was obtained using (220) reflection with MoK α radiation.[90] The result was illustrated in Fig. 18. Dark regions corresponded to those of high microdefect density. It is seen that the dark region consisted of double rings of different brightness which was endorsed in Fig. 3. of another paper reported by Shimizu et al.[89] As was shown in the figure 18, the inner ring was slightly darker than the outer.

In inner ring region, stacking faults were identified to be observed by TEM. Figure 19 shows a stacking fault (extrinsic type) lying on a (111) plane surrounded by Frank partial dislocation having Burger's vector of a/3 $<111>$,[2] accompanying an oxide precipitate as nucleus in the center of stacking fault.[53,89] The oxide precipitate as a nucleus of stacking fault was already formed during the cooling process of the crystal growth and the stacking fault is believed to be formed by an agglomeration of Si interstitials emitted at the SiO_2-Si interface. Thus, these results demonstrate that the occurrence of the R-SF is essentially a heterogeneous growth phenomenon in crystal, thereby, concluding that R-SF is B-SF of which origin is differing from OSF. Thus, we assumed a schematic drawing of the distribution of ring-shaped microdefects in longitudinal cross-sectional view of a Si crystal ingot as shown in Fig. 21.[89] The exact photographs of the longitudinal cross-sectional view of Si crystal ingots were reported by Abe et al.[56-58] in several cases. Thus, figure 21 is merely a speculation, but it is enough to demonstrate that R-SF is definitely B-SF.

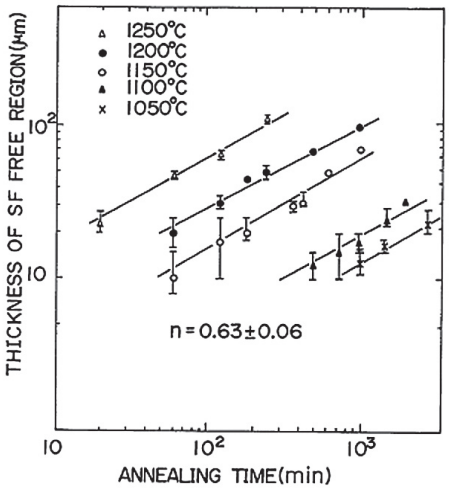

Fig.17. Kinetics of the growth of DZ [Copyright (1978) The Japan Society of Applied Physics].[87]

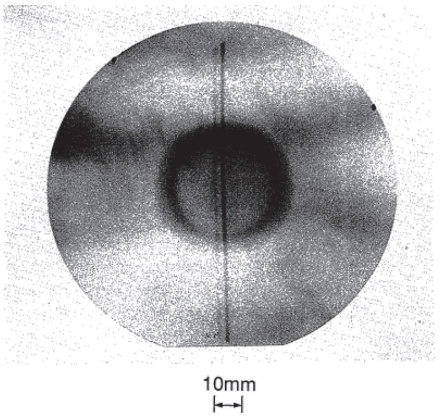

Fig.18. X-ray topograph of R-SF obtained in the same wafer in correspondence of Fig.14 [Copyright (1993) The Japan Society of Applied Physics].[90]

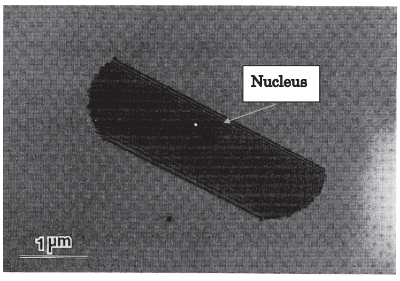

Fig.19. A TEM photograph of an extrinsic type of stacking fault (B-SF) on (111) plane. An oxide precipitate (nucleus) was identified to be existed around the center of the stacking fault [Copyright (1992) The Japan Society of Applied Physics].[89]

In the weak dark area (outside ring) of Fig. 18, rows of prismatic dislocation loops punched out from an oxide precipitate were observed, as shown in Fig. 20. Thus, the difference in contrast between the SPM image and X-ray topograph is considered to be related to the features of individual microdefects.[89]

Figures 22 shows the overall distribution of oxygen concentration ([Oi]) of the wafers before (○) and after(●) the oxidation treatments. During the oxidation at temperatures of 1100 ºC for 58 h, [Oi] was selectively reduced in the ring-shaped region because of oxygen precipitation. This result gave an evidence that nuclei of oxide precipitates existed in the ring-shaped region in the course of ingot growth and cooling in the CZ pulling furnace.

Figure 23 shows the detailed profile of [*Oi*] around the double ring-shaped region, where two corresponding areas are designated by A (stacking faults) and B (oxide precipitates accompanying punched out dislocations). No difference was found in the amount of precipitated oxygen between the two regions. Besides oxygen precipitation, [*Oi*] in the Si matrix is reduced if oxygen atoms congregate at punched out dislocations and form the Cottrell atmosphere.[2] However, it was not clarified how either factors contribute to the [*Oi*] reduction in the present experiment. This inhomogeneity over the whole wafer area aggravates the intrinsic gettering effect.[26] Hence, the deteriorated wafers which contain nuclei of R-SFs should be eliminated when they are used in device processing.

Honma et al.[90] comparatively shows the relationship between the minority carrier lifetime and the crystal defects in Fig. 24. This shows the distribution of photovoltage, minority carrier lifetime, contrast of X-ray topograph, and oxygen concentration. As a matter of course, the SPM image is similar to the lifetime distribution on the basis of the principle of AC SPV.[115-117] The lifetime minima corresponded to the dark regions in the X-ray topograph. The double-ring structure was also reflected in the lifetime as a kink in the distribution. The stacking fault density of about 10^4 cm^{-2} was observed in the surface region of the dark ring on the X-ray topograph by the conventional chemical etching method. On the other hand, only a few defects were observed outside the ring. The interstitial oxygen concentration decreased in these rings as well as the result obtained by Shimizu et al.[89] shown in Fig. 22.

On the other hand, the maxima of minority carrier lifetime were observed at the positions of x = 38 mm and x = 88 mm, as shown in Fig. 24.[90] They corresponded to the bright ring region of the SPM[115-117] image. On the other hand, no crystalline difference was observed in the ring region by X-ray topography. The chemical etching observations revealed that in the longest lifetime region, the lowest amount of microdefects occurred, and these were assumed to be oxide precipitates. Similar but larger microdefects were numerously observed, as well as the stacking faults in the ring-distributed short-lifetime region. Thus it seems probable that the long lifetime results from the oxygen precipitation reduction due to the recombination of interstitial Si (abundant in the outer area of the ingot) and vacancy (abundant in the inner area of the ingot).

Therefore, a ring-distributed short-lifetime region was observed at the same location as the high-density stacking fault region revealed by X-ray topography. Reduction of

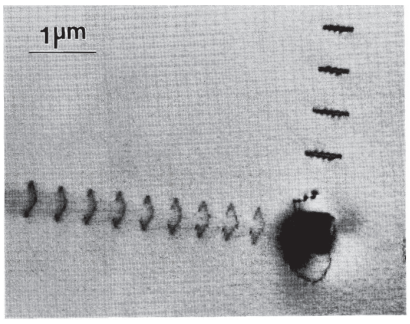

Fig.20. A TEM photograph illustrating rows of prismatic dislocation loops punched-out from an oxide precipitate. The oxide precipitate was identified to be octahedral in shape [Copyright (1992) The Japan Society of Applied Physics].[89]

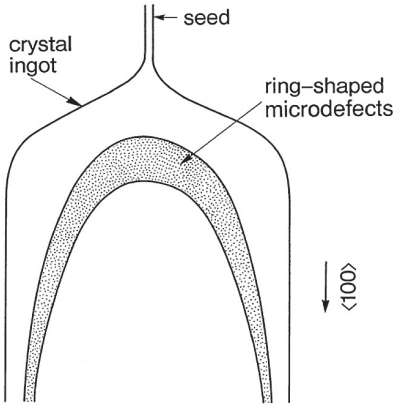

Fig.21. A schematic drawing of the distribution of ring-shaped microdefects in longitudinal cross-sectional view of a Si crystal ingot [Copyright (1992) The Japan Society of Applied Physics].[89]

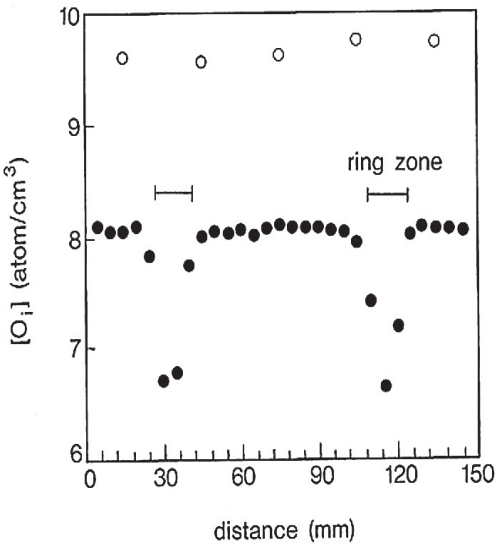

Fig.22. The profile of oxygen concentration in the wafers before (○) and after oxidation (●) at temperatures of 1100 ℃ for 58 h in a dry oxygen ambient. The ring-shaped region is indicated by a solid bar [Copyright (1992) The Japan Society of Applied Physics].[89]

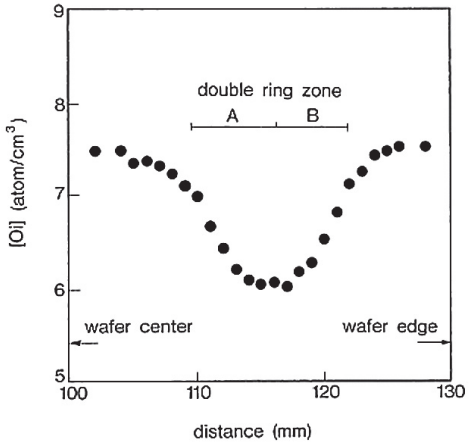

Fig.23. A detailed profile of oxygen concentration around the ring-shaped region denoted in Fig. 22. **A** shows the region of stacking faults and **B** shows that of the oxide precipitates accompanying prismatic dislocation loops [Copyright (1992) The Japan Society of Applied Physics].[89]

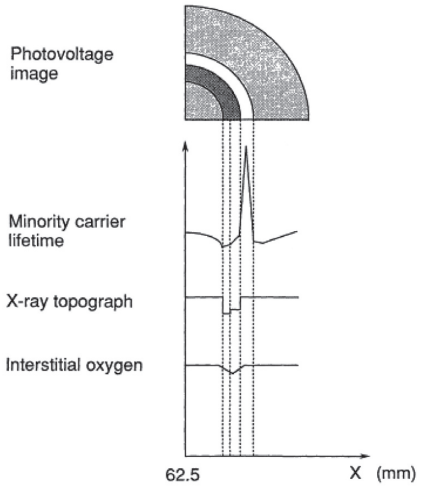

Fig.24. Comparison of minority carrier lifetime with photovoltage image, X-ray topograph and interstitial oxygen concentration [Copyright (1993) The Japan Society of Applied Physics].[90]

interstitial oxygen atoms was also observed in the region.

3.4 Slip dislocation and warpage due to thermal stresses

In 1970s, as pointed out in section 1.3, when dislocation-free CZ Si wafers were thermally stressed at high temperatures in IC processing, slip dislocations happened to be initiated and multiply, thereby, aggravating device performances.[27-34] In the early 1970s, to avoid the introduction of slip dislocations, the radial temperature variation of wafers were necessary to be reduced.[30-32] Thus, slow inserting and slow withdrawal of the wafer batch into and /or out of the furnace kept at high temperatures were performed. Since then several investigators have presented numerical methods for forecasting onset of slip dislocations due to thermal stresses on the basis of analytical simulations.[35-37,119,120,122]

In 1980s, oxygen precipitation became crucial issues to reduce the mechanical strength of heat treated wafers (precipitation softening).[38-43,47] Oxide precipitates accompanying punched-out dislocation and B-SF in the bulk Si played a key role in the occurrence of slip dislocation and/or warpage.[45,48]

Based on wafer samples prepared as shown in Fig. 9, warpage experiments (I)-(II) was performed in the wafers precipitation-treated in a wet oxygen ambient for 16 h at 1000 ℃.[48] The microdefect density in ingots along growth direction was examined with intervals of 50 mm. Sample wafers were preferentially etched and total etch pits were counted before about 40 μm of the surface layers had been removed.

Figure 25 shows the effect of microdefects on the thermal warpage behavior of precipitation-treated wafers; the bowing caused by warpage experiments (I)-(II) is plotted against the microdefect density.[48] The initial bowing of the wafers (approximately 30 μm) generated on slicing the ingots was subtracted from that after the respective heat-treatments. Hence, the warpages indicated the net values arising from plastic deformation during the warpage experiments. In Fig. 25, the observed warpages increased linearly with the logarithm of the density of microdefects, that is, the amount of softening caused by the precipitation treatment was large for the seed-end wafers ([*O*i] was high) and smaller for the tail-end wafers ([*O*i] was comparatively low) (refer to figure 5 in Ref. 48), suggesting that microdefects (oxygen precipitation) were responsible for the softening. The warpage exhibited a pronounced increase when the density of microdefects exceeds 5×10^{9} cm^{-3}. The wafers were then observed by X-ray topography using the (022) reflection. The warpage in the simulated wafers was of the saddle type, because most slips were observed at the periphery of the wafers, where thermal stresses were the highest.

However, we found out specific occasion of an occurrence of slip dislocations in the case of low push in and high pull out of the row of wafers. The temperature of the periphery of wafer firstly decreased than the center, thereby thermal stresses in the center was larger than that of periphery of wafer. Then, the compressive stress in the center caused slip dislocations around the central area in the precipitation-treated wafers with microdefect densities of as much as $2\text{-}5\times10^{9}$ cm^{-3}, for example, at a higher rate of 70 cm/min at 1000 ℃. What counts was that the wafer

deformed in cup-type form. This specific results had a close relationship with an occurrence of dislocations in the compressed region as shown below (Fig. 26).

Furthermore, the warpage dependent on microdefect density obtained in the warpage experiments (I) - (II) were compared with the results by inputting wafers in CMOS processes. Final results gone through all processes were in good agreement with that of Fig. 25,[48] if an initial bowing in fresh wafers (approximately 30 μm) were subtracted from those processed in CMOS as well as in Fig. 25 (refer to figure 10 in Ref. 48).

Observation of etch pits on the (011) cleaved surface in the seed-end wafers showed that dislocations were densely generated at random around the precipitates, suggesting that the precipitates as well as punched-out dislocations function as dislocation multiplication sources when thermal stresses are applied. In the tail-end wafers, the lower density of precipitates caused little slip, and the etch pits of dislocations were thinly scattered in the <Il0> direction. In the precipitation-treated wafers, a larger amount of slip occurred in the compressed region across the neutral plane and a small amount of slip occurred in the tensile region.[132]

Figure 26 shows a cross-sectional view of the wafer deformed into a saddle shape and etch pits of microdefects were revealed by Wright etchant.[118] The upper part of the micrograph corresponds to the concave side of the wafer and the lower part to the convex side. This wafer had a microdefect density of 2×10^9 m^{-3}. Dislocations were delineated as dark pits (indicated by the arrow) and randomly distributed in the concave side. The rodlike etch pits visible in the figure are B-SF that grew by absorbing interstitial Si atoms, which are emitted during the growth of oxide precipitates.[132]

Figures 27 (a) and 27 (b) show schematics of the asymmetrical distribution of slip bands (bundles of slip dislocations) in the Si wafer; Fig. 27 (a) shows a plane view of the etched Si wafer and Fig. 27 (b) shows a cross-sectional view of the area indicted by the dotted line in Fig. 27 (a).[132] These schematics clearly show that when the precipitation-treated wafers were deformed into a saddle shape, most of the dislocation etch pits in the concave side were visible, whereas those in the convex region of the other side were not visible. Sueoka et al.[133] also confirmed that many slip dislocations are generated in the compressed region of (001)-oriented CZ Si (diameter of 150 mm) and that platelet-shaped precipitates produce the nucleation sites for the slip dislocations, as observed with TEM. Furthermore, Shimizu[132] developed a model that explains how slip dislocations multiply and move by bending stresses in saddle-shaped deformed wafers.

In 1980s, for large diameter (4-5 inch or larger) wafers in ULSI devices, sophisticated wafer heat treatments (soft landing technique: see section 1.3) were developed and employed in processes to avoid slip dislocation breakout.

At present in 2016, enlargement of wafer diameter is still pursuing from 300 to 450 mm from viewpoint of cost-effective in device manufacturing. As miniaturization of ULSI device proceeds (half pitch is shrinking from 16 to 11 nm), various assignments are essentially popping up. The problem of process-induced dislocations can be still one of the great concerns in device processes using large diameter wafers.

3.5 Conditions to prevent plastic deformation in large diameter wafers determined by mathematical simulation

In parallel with the experiments in section 3.4, a mathematical thermoplastic simulation based on radiative heat transfers was applied to theoretically predict the presence or absence of slip for wafers from 100 to 200 mm diameter in various process conditions. Figure 28 shows the resolved shear stresses at the periphery of the wafers (slip system S_1; refer to reference 122) calculated for both the heating and cooling processes, plotted as functions of the wafer temperature and the thermal cycles. The process conditions for the calculations were fitted to the experiments. At the same insertion or withdrawal rates, the heating process generates larger thermal stresses than the cooling process, suggesting that the heating process caused heavier plastic deformation than the cooling process did. The direct temperature measurements at various locations on test wafers also showed that the highest stresses appeared at the periphery and the thermal stresses were larger in the heating than in the cooling process at furnace temperatures between 950 °C and 1150 °C. The thermal stresses were relieved first at the periphery, thereby, the generated warpage was of the saddle type. In the case of the saddle-type deformation, the total amount of bowing increased with the higher insertion rates in contrast to cup-type form with higher pull out. The slip lines were observed to be distributed on an extremely fine scale and large in number compared with those of as-received wafers deformed to the same bowing value. The mechanical yield stress σ has been described by the following equation:[121]

$$\sigma(\dot{\varepsilon}, T) = C\dot{\varepsilon}^{1/n} \exp(U/kT) \quad (11)$$

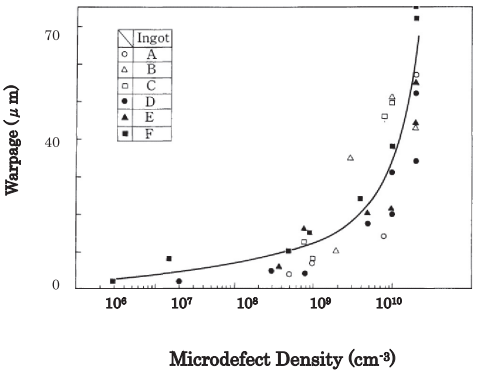

Fig.25. Warpage behavior of precipitation-treated wafers in warpage experiments (I)-(II) plotted as a function of microdefect density. Prior to the warpage experiment, sampled wafers were heat-treated at 1000 °C for 16 h in wet oxygen ambient. The letters A to F represent the crystal ingots used in the present investigation [Copyright (1985) The Japan Society of Applied Physics].[48]

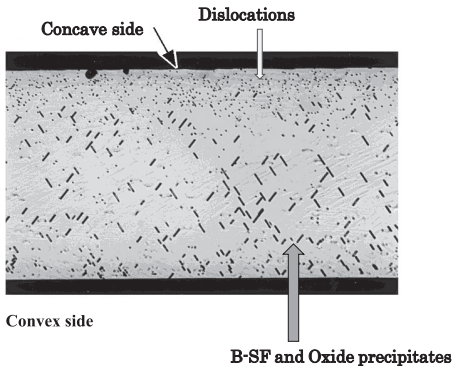

Fig.26. Cross-sectional view of the Si wafers deformed into a saddle shape. The upper part of the rnicrograph corresponds to the concave side and the lower part to the convex side. Dislocations are seen as dark pits in the concave side across the neutral plane [Copyright (2000) The Japan Society of Applied Physics].

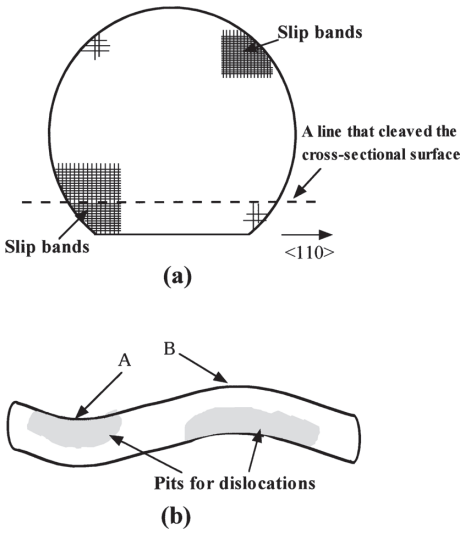

Fig.27. Schematic of the distribution of slip bands of a Si wafer that had been subjected to thermal cycles and then etched. (a) Plane view of the etched Si wafer in which slip bands were formed by bundles of dislocations. (b) Cross-sectional view of dislocation etch-pit distribution at the dotted line in the etched Si wafer shown in (a). Etched pits of dislocations were detected in the concave side of the wafer deformed into a saddle shape [Copyright (2000) The Japan Society of Applied Physics].

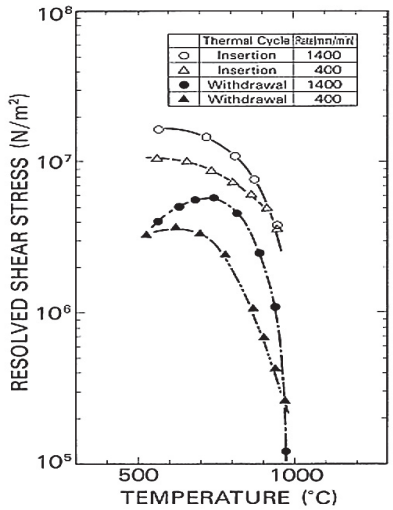

Fig.28. Resolved shear stresses calculated at wafer edges in both the heating and the cooling processes, plotted as functions of the wafer temperature and the insertion or withdrawal rate. The furnace temperature is 1000 °C [Copyright (1988) The Japan Society of Applied Physics].[122]

where U is activation energy of glide movement, T wafer temperature, k the Boltzmann constant, $\dot{\varepsilon}$ strain rate (the time derivative of the initial strain), and n and C constants depending on the material. The yield stress is influenced not only by temperature and strain rate,[121] but also by a marked degree by microdefect density due to oxygen precipitation.[36,48,122] Thus, the yield stress is expected to shift depending on the thermal cycles in device processes. Namely, in device fabrication processing, the critical stresses of processed wafers itself drift due to the characteristics of original strength of the object wafer and heat-treatments in thermal cycles. In order to determine the defect onset conditions, the critical stress σ of the target wafer was estimated by the transient thermal stress curves for the three process conditions (a), (b) and (c), as shown in Fig. 29.[122] The target wafers were those with a diameter of 100 mm processed in CMOS devices.

As shown in equation (5), the yield stress of Si single crystal (as-grown state) has been reported by Alexander

and Haasen.[121] In Fig. 29, as for the wafer with the microdefect density of 2×10^{7} cm^{-3}, thermal stress (a) generated slips, because the thermal stress surmounted the critical stress curve ②. Here, for comparison, the intrinsic yield stress without processings is plotted by the dotted curve ① given by the equation (5).[121] The presence or absence of slips in those wafers was confirmed by etching specimens. Thus, the thermal stress curve (b) corresponded to no slip dislocation condition. As the critical stress is the threshold of the onset of dislocations, it is reasonable to interpolate the yield stress ① between curves (a) and (b), maintaining the exponential dependence on wafer temperature of the curve ①. Thus, the targetted critical stress curve can be shown by curve ②. By the same method, the critical stress curve ③ was obtained for the wafer with the microdefect density of 2×10^{9} cm^{-3}. The strain rate was given as the time derivative of the initial strain in a wafer when the temperatures were around 800 ºC and 900 ºC, and it was estimated to be 9.8×10^{-6} s^{-1} for the curve ②. The exponential constant n was assumed to be 2.6. Then, parameter C was determined to be 6.0×10^{4} N/m^{2} . The estimated critical stress curve ② was in good agreement with that of Matsuba *et* al.[120] Comparing the obtained critical stress with the thermal stress curves, the defect onset could be predicted under various processing conditions.[122]

In order to keep the dislocation-free conditions of those wafers, the thermal stress curves of the target wafers must be below the critical stress curve ②. These process conditions are demonstrated in Fig. 30. At 1000 ºC, the insertion rates were 300 mm/min for 100 mm, 200 mm/min for 125 mm, 150 mm/min for 150 mm and 100 mm/min for 200 mm diameter wafers, when the wafer spacing was 10 mm. This results are able to predict the slip-free conditions from 100 to 200 mm diameter wafers in a row in a horizontal-type furnace on the basis of the calculation of thermal stresses.[122]

As was described before, the prototype thermoelastic wafer model was originally developed by Matsuba et al.[120] for the horizontal-type of furnace. In accordance with wafer enlargement, a vertical-type of furnace was employed in device processes. In order to predict dislocation onset during heat treatments in vertical-type furnaces (200 mm or larger diameter wafer), their model was modified and extended by Shimizu et al.[35,36] The calculated thermal stresses were converted to resolved shear stresses on slip planes (111) in slip directions $<110>$, which are well defined crystallographic directions in the diamond lattice. The critical stress for the initiation of slip dislocations was experimentally deduced on the basis of the mechanical yield stress described by the equation (11),[121] as previously reported in Fig. 29. Once the critical stress is determined, an initiation of slip dislocation depends on whether the resolved shear stress calculated numerically exceeds the critical stress or not. Figure 31 shows the comparison of the resolved shear stress calculated for 300 mm diameter wafers with the critical stress curve. This result gave an evidence of predicting a breakout of slip dislocations in vertical-type of furnaces when 300 mm diameter wafers are input into the device processes even under the prescribed conditions.[35,36]

3.6 Gravitational-induced dislocations in large diameter wafers

In vertical-type furnace, wafers are set horizontally on a supporting jig, often of the point contact type as shown in Fig.11. The wafers bow elastically at the fulcrum of the jig, owing to the gravitational stress originating in bending moment due to their weight. When 200 mm diameter wafers were supported at the jig at around 1200 ºC for several hours related to well-tub diffusion process, a new phenomenon was discovered that slip bands extended from the supported edge along $<110>$ directions with several centimeters length.

Figure 32 shows X-ray topograph of the heat treated 200 mm diameter wafer at 1200 ºC for 3 h in vertical-type of furnace, indicating that slip bands extending along $<110>$ direction were observed at the supporting jig. We have confirmed that this slip propagation was not caused by thermal stresses, but by gravitational stresses, because the processed wafers were heated up and cooled down slow enough to avoid slip dislocations due to thermal stresses.[35-37] This topograph explains that the slip bands were resulted from a collective motion of dislocations. It has been reported that scratching Si surface even at room temperature under a light load of only 2 g caused a small amorphous regions accompanying dislocation.[134] Taking this fact into account, the micro-scratches on wafer surfaces trigger nuclei of slip dislocations when wafers are loaded onto the wafer jig and followed by the subsequent annealing. Upon holding at high-temperature, dislocation multiplies from scratches created at four-point SiC jig, resulting in slip bands. As the wafer diameter is increased, wafer weight increases. As a consequence, in large diameter wafers, stronger mechanical shock and increasing gravitational stress potentially initiate slip dislocations. Macro-roughness on the wafer back surface provides a clue to promote dislocation initiation due to mechanical contact or shock. Thus, these surface irregularities during wafer manufacturing should be also eliminated to

suppress slip dislocations.

In addition to Fig. 32, figure 33 shows an X-ray topograph which was taken to magnify the collective motion of dislocations due to gravitational stresses using (220) diffraction. The Burgers vectors of the dislocations along<110>direction were 60° type in character[121] and some of those dislocations tip were screw dislocations which terminated at the surface.[37]

As pointed out before, wafer weight increased with wafer enlargement due to appropriate thickness augment, thereby, the gravitational stress increased with wafer size. The gravitational stress promoted slip bands if it surmounts the critical stress of a collective motion of dislocations in Si wafers. Therefore, enlarging the wafer to 300 and/or 450 mm in the future will seriously aggravate the problem of the initiation of slip dislocations due to gravitational stresses. To avoid such slippage, several sorts of supporting jigs were devised. One of them was ring-shaped, allowing it to escape from stress concentration at the supporting point. Xin[135] estimated the radius of this ring, to minimize stress components, to be at the ratio of b/R (b = ring radius, R = wafer radius) = 0.7. In that case, he demonstrated that the resolved shear stress in a 300 mm diameter wafer could be reduced to 0.11 MPa.

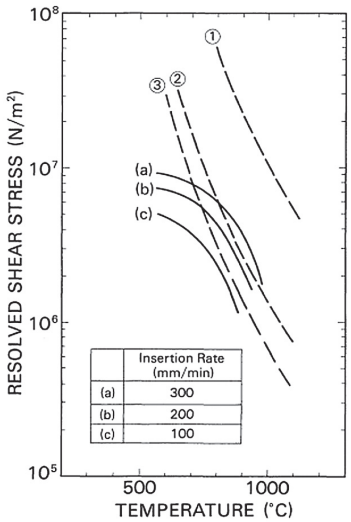

Fig.29. Determination of the critical stress for the precipitation-treated 100 mm diameter wafers. Curve ②corresponds to the critical stress curve for microdefect density of 2×10^{7}cm^{-3} and ③ for 2×10^{9} cm^{-3} [Copyright (1988) The Japan Society of Applied Physics].[122]

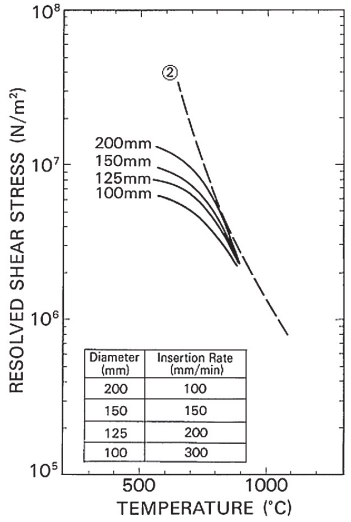

Fig.30. Process conditions to avoid the occurrence of slip dislocations and/or warpage in wafers with various diameters from 100 to 200 mm. The wafer spacing is 10 mm. The broken line shows the critical stress curve ② determined in Fig. 29 [Copyright (1988) The Japan Society of Applied Physics]. [122]

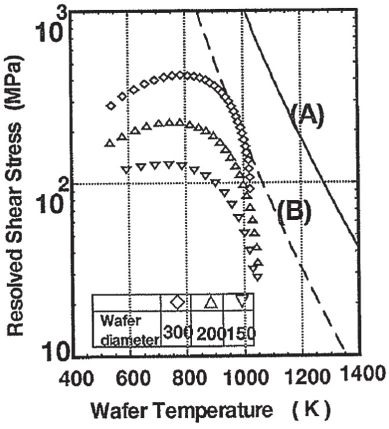

Fig.31. Comparison of the resolved shear stress calculated for 300 mm diameter wafers with the critical stress curve. The curve (A) is plotted by the equation (5) and the curve (B) was obtained as well as done in Fig. 29 (Copyright permission by Mater. Trans. JIM). [36]

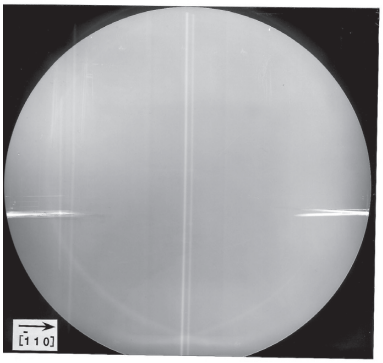

Fig.32. X-ray topograph of the heat treated 200 mm diameter wafer at 1200 °C for 3 h in vertical-type of furnace. Slip bands extending along <110> direction were observed at the supporting jig.

If the combined wafer and ring support are not flat to within several 10 mm or if the ring itself deforms due to its own thermal stress, then the wafer will likely contact only a few points on the ring. In this case, the gravitational stress would be nearly several times greater than for a uniform ring support. Shimizu et al.[36] carried out computer simulation of the development of slip bands due to gravitational stresses using simplified wafer supporting model, where a wafer is set at the center by a solid line. They estimated the gravitational stress to be 0.44 MPa which was larger than that by the ring-shaped jig.

Figure 34 shows the gravitational stress calculated by FEM in 300 mm diameter wafer for three types of wafer supporting jigs.[35,37] One was four-point-type jig, the second was three-point-type jig and the third one was a horse-shoe-type jig (ring-likely shape). Absolute values of the resolved shear stresses are plotted against their distance from the center to the rim of a 300 mm diameter wafer. The analytical soft program in the FEM used for the calculation was commercially available COSMOS/M (SRC Co.). In a numerical calculation, the 300 mm diameter wafer thickness was assumed to be 775 μm. Maximum resolved shear stress was adopted among five independent slip systems as described in 2.5. The maximum process temperature in giga-bit DRAM era was assumed to be around 1000 °C. The critical resolved shear stress for dislocation multiplication condition (0.7×10^6 N/m^2 = 0.7 MPa) at 1000 °C with the microdefect density of 2×10^9 cm^{-3} is drawn by one horizontal line. The gravitational stress obtained in a conventional four-point-jig was likely to overcome the critical stress at the vicinity of point jig, predicting the onset of collective motion of dislocations even if thermal stress is completely suppressed. The horse-shoe-type jig was more successful to reduce the gravitational stress. Thus, the technique of supporting wafers during heat-treatments plays a significant role for suppressing dislocation onset. The critical stress will go down if surface-scratches and micro-cracks introduced during wafer edge rounding assist dislocation generation. Hence, wafer surface should be smooth and strain-free in order to suppress dislocation nucleation. To reduce the contact damage of a wafer with a solid jig in less contaminated manner, a smart wafer handling system is a must, especially for 300 and/or 450 mm diameter wafers.

In conclusion, among three type of jigs, horse-shoe-type jig was found to be successful to suppress slip dislocations at 1000 °C for 300 mm diameter wafers.

In the final analysis, if dislocation-free CZ-Si crystals are subject to high-temperature heat treatments, oxide-precipitates grow accompanying small punched-out dislocation loops which become dislocation multiplication sources under stresses (precipitation softening).[68] The precipitation softening[65,68] greatly reduce the mechanical yield strength. Generally speaking, microdefect is used to include an oxide-precipitate accompanying dislocation loops and stacking faults, thus, as the terminology of Si crystal, "microdefect" is referred to as the indicator of softening of Si bulk crystal. In order to keep dislocation-free state, wafer enlargement necessitates techniques with much slower heating and cooling rates for batch-type processings in order to reduce thermal stresses, and the device miniaturization requires a low-temperature process because of thinner gate oxide and shallower p-n junction

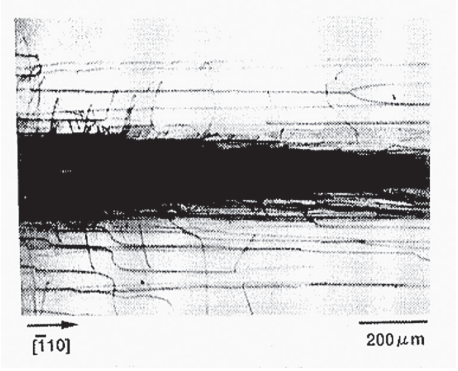

Fig.33. X-ray topograph which was taken to magnify the collective motion of dislocations due to gravitational stresses using (220) diffraction.

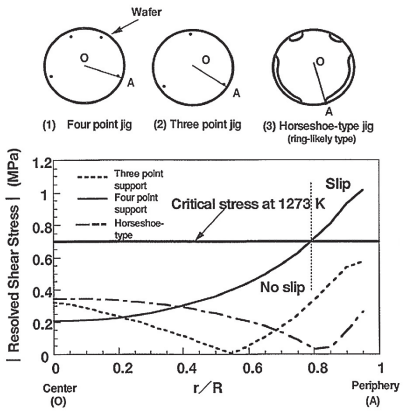

Fig.34. Gravitational stress calculated by FEM in 300 mm diameter wafer for three types of wafer supporting jigs. Absolute values of the resolved shear stresses are plotted against their distance from the center to the rim of a 300 mm diameter wafer (Copyright Permission by The Electrochemical Society).[37]

in ULSI devices. However, the gravitational stress can not be released as long as a wafer is set on horizontal jig, then it becomes crucial for larger diameter wafers. For 300 and/or 450 mm diameter wafer era, a single-wafer-heat-treatment process will be more employed than ever.[136)]

3.7 Intrinsic gettering (IG)

As described in section 1.5 and 2.6, IG sources are oxide-precipitates, punched-out dislocations and B-SF. An elastic interaction between impurities and edge dislocations is, what is called, well-known Cottrell effect.[1)] This impurity locking by dislocations is a key element of IG. Thus, in IG technique, what counts is the formation of DZ and concurrently oxide precipitates in the Si bulk as shown in Fig. 5.

Kishino et al.[138)] proposed a typical IG technique in 1984. Figure 35 shows a schematic of sample wafer treatments which were subjected to three steps of thermal processes successively.[138)] In the second step, the annealing temperature was changed during annealing as shown in the upper part of Fig. 35 (b) where the raising rate of the temperature was varied from 1/min to 5 °C/min. after a holding time. On the other hand, control samples were subjected to the conventional low temperature annealing for 16 hrs at 650 °C as shown in Fig. 35 (b'). The third annealing was carried out as usual in order to enlarge the oxide precipitates in the bulk. The enlarged oxide precipitates and resultant microdefects had a heavy gettering effect. This third annealing corresponded to the total heat treatments in the actual ULSI thermal processes including oxidation and diffusions. The defect density higher than 1×10^8 cm^{-3} in the bulk was suggested to bring a meaningful gettering effect with the procedure. The density is shown in Fig. 36 as a function of both raising rates and holding times of the annealing temperature.

Based on the previous technique, a low temperature annealing longer than 16 hrs was essential for the necessary microdefect density, whereas about 4 hrs were sufficient in this proposed technique. For example, if we use a combination of 3°C/min. and 2 hrs as the raising rate and the holding period, respectively, the annealing time was 3 hrs and 23 mins, where the temperature was raised to 900 °C. Upon raising the temperature during the low temperature annealing, the growth of oxide precipitates was enhanced in comparison with the usual constant temperature annealing. This situation was explained as follows.[138)]

Kishino et al.[138)] described the conventional case in growth of nuclei of oxide precipitates in Fig. 36. If the 650 °C annealing is carried out, the oxygen precipitates whose sizes are larger than the critical size of the precipitate for growth at 650 °C, can grow during the annealing whereas oxide precipitates (m) smaller than the critical size S_1 shrink during the annealing.[71)] When the annealing period is short, a large part of size-number distribution of the oxide precipitates is cut at the critical size T_1 of the subsequent high temperature annealing, and consequently a low density of microdefects are induced by the following 1000 °C annealing as shown with a hatched region in Fig. 36 (a). If the annealing time is extended longer than 16 hrs, oxide precipitates grow in size and the redistribution of the defect occurs as shown in Fig. 36 (b). As a result, a high density of microdefects is induced by the subsequent 1000 °C annealing.

On the other hand, if the temperature is raised during the annealing, the critical size (S_2 or S_3) of the oxide precipitate for growth is also enlarged as shown in Figs. 36 (c) and (d). In Fig. 36 (b), the maximum density is obtained at the size M which was larger than S_1, whereas in Figs. 36 (c) and 36 (d) the maximum density was obtained at S_2 and S_3, respectively. This phenomenon occurs if the expanding speed of the critical size is comparable to the growth rate of the oxide precipitates. It was conjectured that a high density was obtained under the condition that the expanding speed of the critical size was lower than the growth rate of the oxide precipitates. Generally, the growth speed of the oxide precipitates increased largely upon the increase of the annealing temperature. If the temperature was raised discretely, oxide precipitates whose sizes were smaller than the critical size at each discrete temperature shrank during the annealing, whereas almost all the oxide precipitates grew during annealing if the annealing temperature was raised continuously under the condition that the growth rate of oxide precipitates was comparable to the expanding speed of the critical size. Kishino et al.[138)] explained the enhancement mechanism of the microdefect induced by the present low temperature annealing.

Next, the correlation between a wafer warpage and a gettering ability was discussed. As is pointed out in section 3.4, the wafer warpage is detrimental to the ULSI devices, especially, to the micro-fabrication process including lithography. A correlation between the wafer warpage and the microdefect density in the bulk of the starting wafer is shown in Fig. 37 with a broken line[48)] where the wafer warpage was measured after CMOS processing. The wafer warpage vs microdefect density (a broken line) was closely related to that in Fig. 25. Therefore, the wafer

containing microdefects more than 5×10^{9} cm^{-3} is harmful to the ULSI devices. A correlation between a gettering ability and the microdefect density is drawn in the same figure (see Fig. 37) The gettering ability depends on the kinds of species to be gettered and also depends on the kinds of defects induced in the bulk. If the reported data are reviewed, in reference to the number of Ref. 138, they can be approximately drawn with a solid and a dotted line shown in Fig. 37 where each number indicates references number cited in Ref. 138. The dotted and the solid line correspond to the cases where the bulk microdefect is composed of stacking faults and dislocations including rather large sized oxide precipitates, respectively. If one wishes to avoid an unfavorable influence on device parameters by the use of the intrinsic gettering, it is conjectured that the microdefect density should be between 1×10^{7} and 1×10^{9} cm^{-3} where stacking faults are also counted as half dislocations.[138)]

On the other hand, Shimizu et al.[126)] reported an optimum oxygen concentration [*O*i] to getter unwanted impurities on the Si wafer surface. Figure 38 shows the relationship between [*O*i] and the density of OSF on the Si wafer surface (referred to as OSF-S), where their densities were obtained using wet oxidation followed by a successive etching method. In Fig. 38, circles (○), triangles (△) and squares (□) represent the number of oxidation times, i.e. , one, two and three, respectively. Data plotted in the figure include those of wafers sliced from both 100- and 125 mm diameter ingots. As was previously reported, the density of B-SF increased in proportion to [*O*i],[139)] whereas that of OSFs-S decreased with [*O*i] and disappeared when [*O*i] is greater than 9x10^{17} atoms/cm^{3}, as shown in Fig. 38.

As to the [*O*i] less than 9×10^{17} atoms/cm^{3}, repeated oxidations increased the density of OSFs-S, indicating that certain contaminants increased during these processes and these contaminants were responsible for the nucleation of OSFs-S. This result shows that the lower [*O*i] causes a smaller number of microdefects in the bulk crystal, thereby reducing the gettering efficiency. The TEM photograph gave an evidence that OSFs-S frequently grew from the nuclei which were possibly clusters of impurities ungettered in the bulk,[140,141)] as shown in Fig. 39. Metal impuritiess and/or fluorine[142)] on wafer surface are possible as the nucleation sites for the OSFs-S.

In Fig. 38,[126)] the relationship between [*O*il and the warpage caused by the thermal stress cycles was represented by a plus sign.[49)] When wafers containing higher [*O*i] are subject to heat treatment in device processing, precipitation softening easily occurs. Such wafers are susceptible to warpage due to thermal stresses.

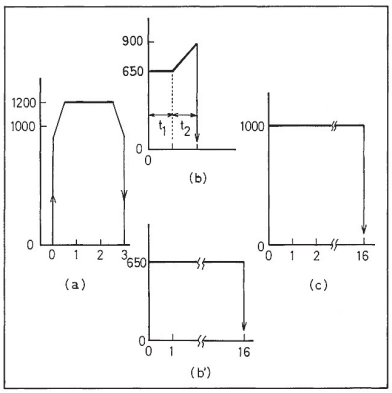

Fig.35. Temperature cycles of three kinds of-annealing. (a) is the first high temperature annealing for 2 hrs at 1200 ºC for the formation of a DZ. (b) and (b') are low temperature annealings for the nucleation of the oxygen precipitates followed by growth in the case of the proposed and the conventional technique, respectively, where t_1 is the holding time. (c) is the third annealing for 16 hrs at 1000 ºC [Copyright (1981) The Japan Society of Applied Physics].[100)]

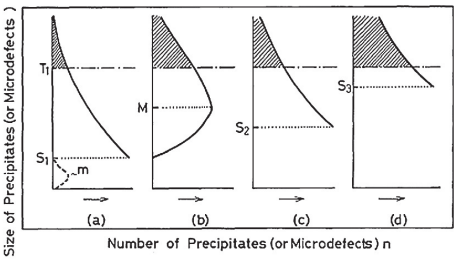

Fig.36. A size-number distribution of precipitates (or microdefects) after annealing in the case of the conventional (a and b) and of the proposed (c and d) technique, respectively. S_1 and T_1 are critical sizes of the precipitate for growth at 650 ºC and at 1000 ºC, respectively. Each hatched region shows the microdefects induced by 1000 ºC annealing after the low temperature annealing. S1 and S3 show critical sizes at temperatures between 650 ºC and 900 ºC [Copyright (1981) The Japan Society of Applied Physics].[100)]

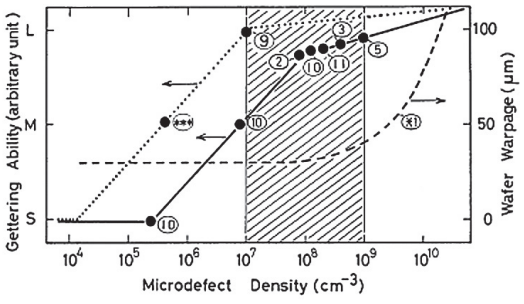

Fig.37. Gettering ability as a function of bulk microdensity and a correlation between wafer warpage and the density. L, M, and S show large, medium, and small gettering ability, respectively. A solid (dotted) line shows a correlation between a gettering ability and a dislocation (B-SF) density,whereas the broken line shows a correlation between a wafer warpage and a defect density. Each number circled shows the number of a reference paper cited here [Copyright (1981) The Japan Society of Applied Physics].[100)]

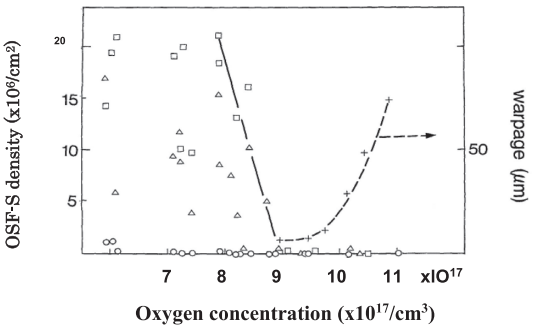

Fig.38. Variation of OSF-S as a function of [Oil. The circles (O), triangles (△) and squares (□) correspond to one, two and three oxidation times. The plus (+) shows the relationship between [Oi] and warpage caused intentionally by heat cycles based on in Fig. 10 of Ref. 49 [Copyright (1993) The Japan Society of Applied Physics].[126)]4

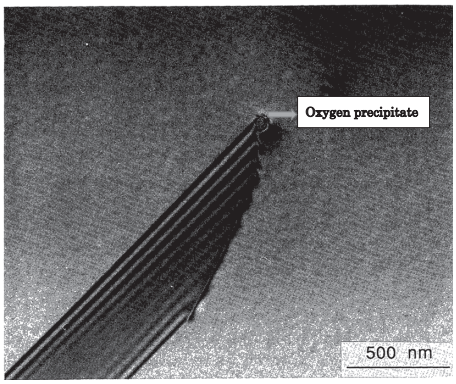

Fig.39. TEM image of an OSF-S with the impurity cluster [Copyright (1993) The Japan Society of Applied Physics].[126)]

It is observed that the critical [*O*il required to reduce warpage should be less than 10×10^{17} atoms/cm^3. Hence, the optimum [*O*il required to suppress OSFs-S in device processing was postulated to be between 9- and 10×10^{17} atoms/cm^3.

3.8 Summary of influence of COP defects in ULSI device in 1996-2000 and thin-film epitaxial growth

As described above in section 1.6 and 2.7, COP_S on wafer surfaces have been identified as truncated octahedral voids in which vacancies coalesce during CZ crystal growth and are frozen into the crystal. COP_S about 0.1-0.3 μm in size cause irregular thickness variations in the oxide film, and give rise to isolation leakage between memory cells in DRAM devices that follow the 0.3 μm design rule in 1996-2000.[109,143-145)] In 1998, Muranaka et al. analyzed the influence of COPs in DRAM device (0.3 μm design rule) characteristics.[143)] Then, Shimizu et al.[144)] presented in proceeding of symposium of the 195th electrochemical society of spring meeting at Seattle in 1999 (Defects in Silicon III) under the title of effects of surface defects (COPs) on isolation leakage and GOI in MOS-ULSI devices and cost effective p-/p- epitaxial wafers. Muranaka, Shimizu and coworker's results[143-145)] are summarized in the following.

On the other hand, Shimizu et al.[146,147)] already reported that even when COP_S existed on the wafer surface, a 0.3 μm thick epitaxial layer was sufficient to raise the GOI in p-/p-structures, and a 1 μm thick epitaxial layer decreased the isolation leakage to acceptable levels.[144-145)] The prototype p-(n-)/p-(n-) thin film Si epitaxial wafers have several advantages, which include the ability to fabricate devices by conventional design techniques in CZ-Si (p- substrate) wafers and also avoidance of auto-doping from the p+ substrate.[146,147)]

The density of COP_S can be controlled by optimizing the growth rate (V) and the temperature gradient (G) at the liquid-solid interface during CZ growth (see section 3.1). The demand for COP reduction during crystal growth has been become more crucial as design rules for devices are changed into below 0.25 μm around in 2000.

On the other hand, epitaxial wafers are promising to decrease the density of oxide defects in highly packed devices and in multiple thickness gate processing, but the cost of epitaxial wafers was approximately 1.5 times higher than that of conventional min or-polished CZ-Si wafers in those days. The continual pressure to reduce the cost of metal oxide semiconductor (MOS)-ULSI devices will cause the cost of epitaxial wafers to approach that of mirror-polished CZ-Si wafers.[146,147)]

For ease in the formation for MOS microcircuits, in contrast to wafers with p-/p+ structure, epitaxial wafers with p-/p- structure are easily replaced by using conventional CZ mirror wafers (p-).[146,147)] However, heat-treatments around 1000 ℃ reduce the number of nuclei of oxide precipitates in the CZ-Si substrates, resulting m the p-/p- epitaxial wafers with less gettering capability for undesirable impurities.[146,147)] The evaluation method of gettering capability was also a significant work to develop less expensive wafers with high performance.

Figure 40 shows a plane-view SEM image of the COP imprint between adjacent cells under a field-oxide film and the adjacent word line, taken after removing the field oxide. The hole-like pit is the COP imprint, and the word line is indicated by the arrows.[143-145)]

Figure 41 shows a cross-sectional SEM image of the defective field oxide film from another direction. Compared

with the normal shape, the field-oxide film became thinner at the COP imprint. [143-145)]

In LOCOS processes, the nitride film remaining at the bottom of COP_S after dry etching caused the field oxide to grow as shown in Fig. 42. As reported by Muranaka et al.[143)] and shown in Fig. 42 (c), ion implantation pushed boron ions into deeper regions, through the field oxide that was irregularly thinned by the existence of COP_S. Therefore, the area implanted by boron ions did not act as a channel stopper, and correspondingly, the isolation characteristics significantly degraded. Furthermore, the phosphorus ions that formed the source and drain were also driven into the substrate through the thinned area, just outside the word line [Fig. 42 (d)]. The concentration of doped phosphorus therefore increased in that area and, consequently, the degradation of MOS transistors further accelerated. Muranaka et al.[143)] showed that leakage current on the substrate of defective cells caused by COP_S significantly increased compared with non-defective cells. A Simulation of the leakage current at the thinning point showed good agreement with their measured results.[143)]

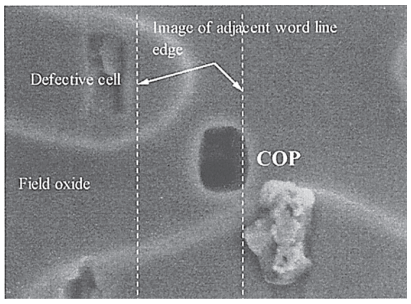

Fig.40. Plane-view SEM image of the COP imprint between adjacent cells under the field oxide film and the adjacent word line (Copyright Permission by The Electrochemical Society).[145)]

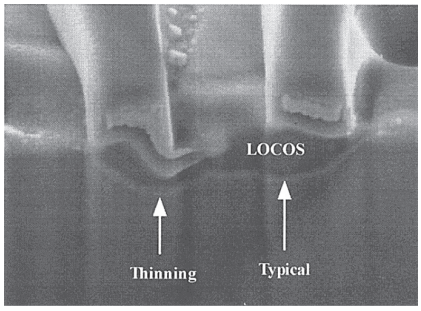

Fig.41. Cross-sectional SEM image of the COP imprint which caused thinning. A typical LOCOS shape is also shown (Copyright Permission by The Electrochemical Society).[145)]

In the next step, we described improvements of GOI in the prototype p-/p- thin-film Si epitaxial wafers. Figure 43 shows the oxide defect density normalized by the oxide defect density for mirror-polished CZ-Si wafers *vs*. the epitaxial layer thickness using test devices with a LOCOS isolation structure, when [*O*i] of the Si substrate varied from 7.4×10^{17} to 9.8×10^{17} atoms/cm^3. The CZ denoted in the figure refers to the results for conventional CZ-Si wafers. As the epitaxial layer thickness was increased from 0.01 to 0.1 μm, the normalized ratio of oxide defect density decreased from 1 to 0.2 and approached a constant value of about 0.03 for a film thickness greater than 0.3 μm. Thus, the prototype p-/p- epitaxial thickness had been determined to be 1 μm.[146,147)] The CZ-Si substrate with COP_S was covered by a defect-free thin-film epitaxial layer, thereby reducing the oxide weak spots by flattening the comers of truncated octahedral voids (COP_S). However, the unidentified defects in the epitaxial layer measured by optical shallow defect analyzer (OSDA)[148)] increased during heat-treatrnent, indicating that an epitaxial layer thicker than 1 μm is necessary to ensure defect-free regions by preventing the occurrence of oxide precipitates caused by oxygen diffusion from the CZ-Si substrate.

Considering the anticipated future use of p-/p- epitaxial wafers in MOS-ULSI devices, an improvements will be essential for p-/p- epitaxial wafers as discussed in the following section.

3.9 Heavy metal impurity control and development of analytical methods

In 1990s, metal contamination control and evaluation techniques on wafer have been drastically developed. The wafer cleaning procedure in Si device fabrication usually employed a combination of RCA solution (alkaline and acid)[107)] and an aqueous hydrofluoric acid (HF) solution with a small additional hydrogen peroxide including surfactant.[149)] Appreciable amounts of metal impurities (10^9-10^{10} atoms/cm^2) still remain on the cleaned Si wafer surfaces. Hence, the cleaning and its evaluation are major concerns and extensive investigations are being conducted. By improving contamination diagnosis during device processing, we expected to get higher yields in ULSI. Thus, it was necessary to accurately measure ultra low levels of contamination on both incoming and processed wafers. In 1990s, high resolution analytical methods which can sensitively detect traces (ppt) of the contamination have been reported. A typical method was ICP-MS with a double focusing magnetic sector mass analyzer.[150,151)] This kind of high resolution analytical instrument put stringent demands on the sampling method intended to extract specific elements in a clean environment. The vapor phase dissolution (VPD) method combined

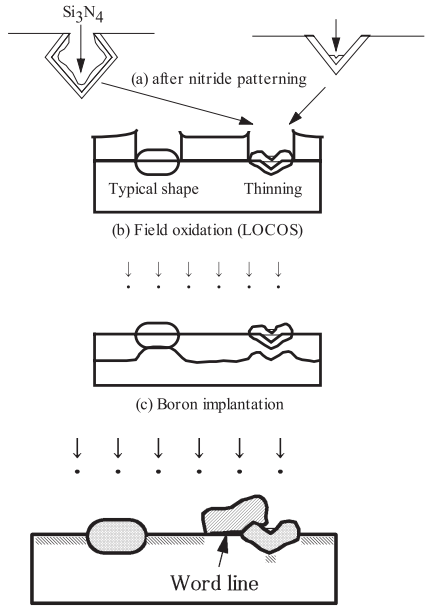

Fig.42. Illustration of the bad effects in MOS devices caused by thinned LOCOS field oxides due to COP_S: (a) COP_S in which the residue of nitride mm (Si_3N_4) after dry etching partly ml the well of the COP_S, (b) LOCOS field oxide growth constrained by the residue of nitride films, (c) boron ion-implanted areas through irregularly thinned oxides, (d) phosphorous ion implanted regions in thinned oxides (Copyright Permission by The Electrochemical Society).[145]

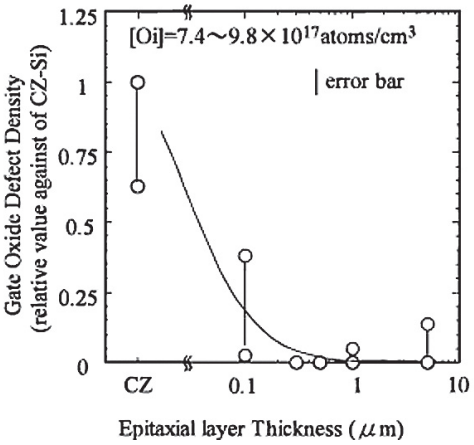

Fig.43. Oxide defect density determined for test devices with LOCOS field edge structures *vs*. epitaxial layer thickness (Copyright Permission by The Electrochemical Society).[145]

with atomic absorption spectroscopy (AAS),[152] ICP-MS[153] and total reflection X-ray fluorescence (TRXF),[154] have been proposed to detect metallic contaminants on Si wafer surfaces. As for sampling method of VPD, one side of the Si wafer was exposed to HF vapor in a clean, closed chamber. The HF vapor decomposes the native or thermal oxide layer on the wafer and collects a droplet of acid as a sample.

From 1990s through 2010s, metallic contaminations on oxide surface were reported to affect device characteristics and they increased during air exposure. Hence, there appeared an increasing demand to analyze separately between oxide surface and oxide bulk in a simplified way and with high throughput in a clean environment. In addition, purification of chemicals and water have been improved year by year. Furthermore, new closed wafer cassette and mini-environment system are coming to reject contamination in 2016.

In the days of 1990s, in order to meet the various requirements, a PEM which Ishiwari et al.[127,155,156] developed can be one of the strong tools. Figure 44 shows the procedure of the PEM where a sample wafer is packed in a clean double-layered polypropylene bag with hot water or in a clean *teflon* bag with an acid solution (HCl/H_2O, HF/H_2O, $HF/HNO_3/H_2O$ including surfectant).[156] This method has already been utilized to monitor impurities (anion, cation, metal) for various purposes.[155,156] The features of the PEM were summarized as follows: (1) an extraction of impurities on both front and back surfaces of the wafers can be done simultaneously, (2) the environmental pollution during extraction can be minimized once sample wafers are enclosed in the bags, (3) an extraction can be applicable for both anion and cation impurities in addition to detrimental metal impurities, (4) it is easier to simultaneously treat many specimens in the same water bath.[155]

Figure 45 shows the heavy metal concentration on Si wafer surfaces for three wafer vendors, respectively by A, B and C in 1990s.[156] Ten wafers of each vendor were analyzed, and measured concentration were averaged after removing the highest and lowest values. The scattering of the data was within ± 5 percent. For all three vendors, the detection limit (DL) of the combined improved PEM and ICP-MS was always lower than the measured concentration of the impurity on the wafers. Because of the need of ultra-trace analysis in cleaned wafers, ICP-MS with high accuracy turned out to be a useful technique to monitor remaining impurities on the surface of incoming wafers on regular basis. Moreover, the device characterization proved that lower trace elements on the surface of

the wafers fitted satisfactorily the present densely packed MOS devices, because one of the detrimental impurities of Fe accumulated up at the SiO_2-Si interface, resulting in degradation of electrical characteristics.

Based on the prototype PEM method,[155,156] we have tried to obtain various results related to depth profile of Al and Fe impurities in thermal oxide.[157,158] Because more crucial demands emerged to separately measure the metal impurities between the oxide surface, SiO_2 film and Si-bulk crystals. Therefore, the prototype PEM method was improved to separately extract impurities at the oxide surface, within the oxide and SiO_2-Si interface, using the same sample, respectively.[127] Then, taking an example to pick up, Cu, Fe and Al,[159,160] some wafers were deliberately contaminated by utilizing Cu, Fe, and Al ion solution [standard 1000 ppm (1 mg/ml)] into the RCA alkaline solution. The final ion concentration in the RCA rinsing solution was 1 μ g/ml. Then, the three samples were oxidized at 1000 ℃ for 60 min and analyzed by means of the improved PEM and ICP-MS.

The improved PEM[127] was suggested in the following. For the first hand, three types of solutions ([I] HCl/H_2O, [II] HF/H_2O and [III] HF/HNO_3/H_2O), were prepared and replaced one after another in one bag. The experimental steps were as follows: [I] ; sample wafers were packed in cleaned *teflon* bags with 10 ml of the hydrochloric acid solution (HCl:H_2O=1:1000) and kept at about 95 ℃ for 30 min in water bath. This treatment is directed specifically to extracting the metal impurities at oxide surfaces because HCl does not dissolve SiO_2. After the first extraction was done, [II] ; the sample wafers were enclosed in another cleaned *teflon* bags again using the HF solution (HF:H_2O=1:1000) at about 95 ℃ for 30 min. In this step, impurities in the oxide is dissolved into solution, but the solution does not dissolve Si bulk. Then, [III] ; the sample wafers were put into the cleaned *teflon* bag with the acid solution (HF:HNO_3:H_2O=1:1:100) at about 95 ℃ for 30 min. During the last extraction, the Si bulk surface was etched away to a depth of about 0.4 μm. These sample solutions were introduced into high resolution ICP-MS. Hence, those impurities were analyzed each for [I] ; the oxide surface, [II] ; the oxide and [III] ; the bulk of Si.

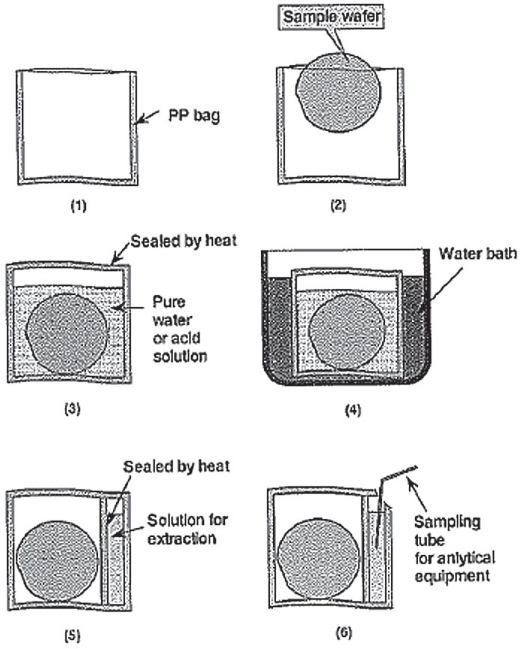

Fig.44. Procedurag e for impurity sampling at wafer surface by a PEM shown as follows in six steps; (1) cleaned PP (PP: polypropylene), (2) a sample wafer is put in PP bag, (3) an acid solution (HCl/H_2O, HF/H_2O, HF/HNO_3/H_2O including surfectant) is put in *teflon* bag, and the *teflon* bag is closed and sealed by heat, (4) a sample is heated in a water bath (95 ℃ for 30 min), (5) after extracting impurities, wafer and solution are separated and sealed by heat, (6) extracted solution is taken out and introduced into ICP-MS (Copyright permission by Mater. Trans. JIM).[156]

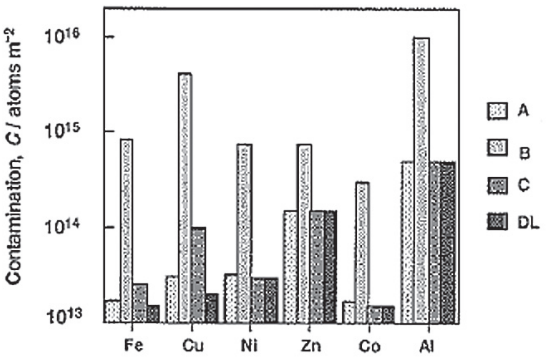

Fig.45. Heavy-metal contamination of the surfaces of Si wafers from three vendors, represented by A, B and C. DL means the detection limit of ICP-MS (Copyright permission by Mater. Trans. JIM).[156]

4. Conclusion

This report described a remarkable progress in silicon (Si) crystal technology with an aim of advancements in electrical performances from integrated circuit (IC) through ultra-large-scale-integration (ULSI) device era. Since 1960s, an advent of an epoch making IC device needed to control crystalline defects in Si crystal grown by Czochralski (CZ)-pulling method, inspiring researchers to grow dislocation-free single crystals and also to reduce process-induced defects such as thermally-induced and/or gravitational-induced dislocations, oxidation-induced stacking faults (OSF), crystal originated particles (COP_S) and deleterious impurities by gettering as wafer

enlargement and the miniaturization of device progressed until nowadays.

A method to experimentally control OSF in N_2 annealing "post oxidation annealing" and to avoid slip dislocations due to thermal stresses were reviewed and summarized. The post oxidation annealing technique eliminated OSF and formed denuded zone (DZ) underneath SiO_2-Si interface, thereby the technique may be a crack of dawn of intrinsic gettering (IG). To reduce slip dislocations due to thermal stresses in ULSI device processes, what counts was to control an optimum microdefect density in order to maintain less warpage. The microdefect density should be less than 5×10^9 cm^{-3} to prevent permissible range of warpage in ULSI device processes. Moreover, it was summarized that mathematical calculation methods were successfully established to predict the occurrence of thermal stress- and/or gravitational-induced dislocations in 200 and 300 mm diameter wafers.

A mechanism of point defects (vacancy and interstitial) clustering and secondary defects of oxygen precipitates including punched-out dislocations and staking faults during CZ Si crystal growth was reviewed. Such microdefects were found to cause electrical failure in Si devices, and concurrently oxygen precipitates and DZ in Si bilk gave rise to benefits to device characteristics by capturing unwanted impurities from p-n junction area which is called IG. Many researches related to IG were reviewed and specific experimental results were described. At the same time, suitable oxygen concentration [*O*i] in CZ Si wafer to getter surface impurities was determined. The optimum [*O*i] required to suppress OSFs-S in device processings was postulated to be between 9- and 10×10^{17} atoms/cm^3.

COP_S on Si wafer surfaces, which reportedly are truncated octahedral voids in Si crystal ingot, caused local thinning of the field oxide, and thus increased the isolation leakage between memory cells in ULSI devices with 0.3 μm design rule. In the prototype p-/p- thin-film Si epitaxial wafers, a 1 μm layer thick film was sufficient to cancel such detrimental COP_S, and to improve the gate oxide integrity.

However, essentially, sophisticated CZ crystal growth could overcome this crucial assignment by controlling point defects such as vacancy and/or interstitial. Although IG technique improved to suppress the deleterious effects of impurity contamination at wafer surfaces, the impurity contamination itself was found to be fatal issues for ULSI devices, thereby, essentially, cleaning technology and analytical techniques were remarkably developed. Finally, the point defect dilemma among many researchers during Si crystal growth from 1982 through 2016 was reviewed.

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総合教育編

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ヴァルドルフ教育における「12感覚」論

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“The Twelve Senses” in Waldorf Pedagogy

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Abstract

This paper examines how “the twelve senses”, proposed by Rudolf Steiner, is accepted in Waldorf Pedagogy. Firstly, it picks up one of Steiner's lectures on “the twelve senses” and summarizes his theory. And then, it takes up the theory of education by Stefan Leber, one of the most important pioneers of the German Waldorf school movement, in order to explain the relationship between “the twelve senses” and education. Finally, this paper reaches the four main points as follows:

１．Steiner's “twelve senses” has percolated to every level of Waldorf education.
２．Steiner's “twelve senses” maintains that a human being is a unified organism. All sensory organs are closely related to each other to perceive.
３．Steiner's “twelve senses” assumes one aspect of desirable human development. Each sensory group and organs has predominate developmental stages respectively.
４．Steiner's “twelve senses”, as a basic principle, has become a course of action in the Waldorf School.

Key words: Rudolf Steiner, The Twelve Senses, Waldorf Pedagogy, Waldorf School

1　はじめに

本稿では，ヴァルドルフ教育において重要概念であるとされる，「12感覚」に焦点をあてる(註1)。「12感覚」は，ルドルフ・シュタイナー（Rudolf Steiner）が提唱したものである。ヴァルドルフ教育関係者の一人ヨハネス・キールシュ（Johannes Kiersch）は，シュタイナーの「12感覚」について次のように書いている。「シュタイナーの感覚論は，[略]彼の教育的人間学の中核とみなすべきものである」（Pädagogik 29）（前は文献の略称，後は頁数，以下同様）。ヴァルドルフ教育の入門書と位置づけられているこの書において，キールシュは，「12感覚論」がヴァルドルフ教育の核心部分にあるとみなしている。

「12感覚」は，シュタイナー「霊学Geisteswissenschaft」に基盤をもつとされている。しかし，現実の教育，教育実践を問題にするとき，その基盤にある「霊学」まで遡る必要はないであろう。シュタイナーの「12感覚」論は，教育論として，あるいは教育実践に取り入れるための視点で再解釈されているはずだからである。このような基本的スタンスに立って，シュタイナーの「12感覚」の概要を確認し，それが，ヴァルドルフ教育においてどのように論じられているかを検討する。

本稿ではまず，シュタイナーの「12感覚」論を取り上げ，その概要を提示する。次に，シュタイナーの「12感覚」がヴァルドルフ教育の中でどのように論じられているかの一例として，シュテファン・レーバー（Stefan Leber）の教育論を取り上げる。それによってヴァルドルフ教育における「12感覚」の位置づけを，読み取ることができるだろう。「12感覚」論は，ヴァルドルフ教育において有効なだけでなく，一般的な教育論，教育実践に対して有用な示唆を与えうるものであることを最後に指摘する。

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2　講演における「12感覚」論の全体像
―「人間の12の感覚」―

シュタイナーの「12感覚」に関しては，シュタイナーの著作物やヴァルドルフ教育研究の成果や情報等を専門に出版している*Freies Geistesleben*社から，*zur sinneslehre*が出ている。この本には，「12感覚」に関するまとまった唯一のテキストである『魂の謎について』の中の当該箇所(註2)や，「12感覚」に関するシュタイナーの幾つかの重要とされる講演が収録されている。彼の感覚論の全体像を把握するには格好の文献である。ここでは，ドルナッハで行われた1921年７月22日の講演（「人間の12の感覚」）を取り上げる。『魂の謎について』の出版が1917年であり，この講演までにシュタイナーの感覚論が，より整理され，明確なものになった。ここでは，「12感覚」の全体像把握に努めることにしたい。

シュタイナーは，講演の冒頭で今日の感覚に関する研究が皮相的なものであると批判する。その例として，「自我感覚」が初めに取り上げられる。一般的な自我のとらえ方は，誤解にみちているという。自分に自我があることが前提にされ，他者にも自我があると仮定し，さらに他者の外見等から自我の内容が類推されるのが一般的だという。シュタイナーは，次のように続ける。

この類推は，まったく役に立ちません。なぜなら，私たちが直接外界に向かい，外界のある領域を視覚で捉えるのとまったく同じように，他者の自我が私たちの体験領域に直接入り込むからです。私たちに視覚があるとみなすならば，自我感覚もあるとみなさねばなりません。（zwölf 9f.）

引用文の中に，シュタイナーの感覚のとらえ方が表現されている。感覚は，外界の事象を受け取る働きをするものである。感覚は，受容的なものである。視覚が外界の刺激を受け取るのと同じように，他者の自我も，外見などから類推するのではなく，感覚で受け取ることができるものであるという。「自我感覚」も例外ではない。他者の自我は，「自我感覚」によって直接知覚される。

他者の思考を知覚する「思考感覚」についても，「自我感覚」と同様の説明がされている。

［略］他者の思考を知覚することと，本来的な思考とを区別しなければなりません。［略］確かに他者の考えが知覚される場合には，この考えを理解するために，既に持っていたものと関係づけるために，私たちは思考しなければなりません。だがこの思考は，相手の思考を知覚することとは全く別なことなのです。（ebd. 10f.）

「思考感覚」は，感覚であるがゆえに，他者の思考を受動的に知覚する。それに対して思考は，知覚したものを理解するために行われる。知覚内容と，それに対する思考活動は区別される。

さてこの「12の感覚」において，特筆すべきことの一つは，シュタイナーが「12感覚」をその機能に即して３分類していることである。そして諸感覚を「思考」「感情」「意志」に対応するものとしている。この３分類からなる「12感覚」は以下のように示されている。（ebd. 28）

明確な外部感覚		外部的―内部的感覚		明確な内部感覚	
表象系	自我感覚	感情系	熱感覚	意志系	平衡感覚
	思考感覚		視覚		運動感覚
	言語感覚		味覚		生命感覚
	聴覚		嗅覚		触覚

上に示されている「12感覚」が，人間がもつ完璧な感覚とされるものである。挙げられている感覚とその並び順は，『魂の謎について』におけるテキストとまったく同じである（rätseln 147）。

この中で，表象系，感情系，意志系とあるが，シュタイナーは，『教育の基礎としての一般人間学』の中では，それぞれ「認識感覚Erkenntnissinne」，「感情感覚Gefühlssinne」，「意志感覚Willenssinne」とも表現している。それぞれ主に思考（表象），感情，意志と関係する感覚のグループであることを意味する（註３）。

「外部感覚」は，外部刺激を受容するが，自覚的に受け取る器官である。但し，自覚の程度は人間の発達段階により異なり，成長するに従いしだいに自覚的になる。「内部感覚」は，自分自身の内面を感じる器官を意味し，意識的な感覚ではなく，「意識下」の感覚である。「外部的―内部的感覚器官」は，外部の刺激を自覚的に受け取る機能と，自分の内面を感じる両面の機能を合わせもつ。

さらに「12感覚」は，主に「表象」と関係する感覚，「感情」と関係する感覚，「意志」に関係する感覚に分類される。表象系に分類される感覚は，同時に明確な「外部感覚」として分類される。つまり，外部刺激を受け取る感覚として考えられている。感情系に分類される感覚は，外部刺激を自覚的に感覚する器官であると同時に，「意識下」において自分自身の内面の状態を自覚する器官でもある。３番目に分類される感覚は，意志と結びついているものとされている。そして，「意識下」において自分自身の内面の状態を感じる器官である。

このような分類にもかかわらず，注意すべきことがある。それは，諸感覚を以上のように分類し，機能も異なるとしながら，諸感覚が相互に関連することで初めて，各感覚の働きが可能になることが強調されていることである。「思考」「感情」「意志」に関しても同様で，相互に有機的に結びつくことで初めてそれぞれが働くとされる。

3　S.レーバーの「12感覚」解説　(1)

シュタイナーの「12感覚」を，教育論の中で解説している一人がシュテファン・レーバーである。レーバーは，ヴァルドルフ教育の全体像を明確に示す，まとまった教育論を著している。この中から「12感覚」について主に論じられている箇所を取り上げる。本節は，第一部「人間の本性」の部分である。

レーバーは，シュタイナーがフランツ・ブレンターノ（Franz Brentano）心理学との取り組みから，「志向的関係」の観念を引き継ぎ，「魂」の特性に目を向ける観点を得たとしている（Menschenkunde 110）。彼はそう指摘し，物質的諸現象と異なる心的諸現象の特性について，次のように書いている。

心的諸現象は，直接的な内面的知覚を通して，直接的な実在の根拠となる直接的明証性を得る。［略］思考において志向的関係は，（志向的）対象それ自体を理解することにある。私たちは，対象と距離を保ち，それを十分に研究し，観察し，イメージする。感情において私たちは，対象を欲するか避けるかし，好感か反感をもつ。意志において私たちは，対象を欲し，自分のものにし，作り上げる。そうすることで魂は，周囲のもの，あるいは自分自身と絶えず関わる。（ebd. 110f.）

「魂」すなわち「心的諸現象」は，「思考」し，「感情」をいだき，「意志」をもつという，その基本的特性を確認する。そしてレーバーは，シュタイナーの「12感覚」研究によって，「感情」の世界の重要な視点を得られるという。

既述のように「思考」「感情」「意志」は，相互の関わり合いなしには働かないが，レーバーの著書では，主に「感情」領域において「12感覚」が中心的に解説されている。彼は，シュタイナーの分類をそのまま踏襲し，先の表の右下の「触覚」から左上の「自我感覚」へと順に解説が続く。

⑴ 「意志感覚」に基づく感情

レーバーが「身体感覚」と呼ぶ，「意志感覚」が関係するのは，自分の身体とその中で起こるプロセスの知覚内容である。「触覚」が最初に取り上げられる。

> 触覚的接触，触覚を通して，すべての未知の知覚内容と共に，同時に自身の経験が伝えられる。柔らかいものや硬いものといった，形のあるもの，対象物の感覚内容がそれによって生じる。それに続いて起こる感情は，親密，親しい人として，また安心感としても言い表すことができる。［略］触覚による感覚内容から，存在感，同じく活力体験が生まれる。触覚は，重さの感覚をも伝える。これには，重圧，ストレス，憂鬱や意気消沈の感情が結びついている。（ebd. 123）

レーバーの説明で共通していることは，「感覚」が外的情報を知覚すること，そして同時に，「感覚」による知覚内容によって内面に引き起こされる，特定の感情が挙げられていることである。「触覚」は，人との接触を通して，「親近感」や「安心感」を味わったり，「親しい人」を感じたりする。その一方で，「重圧」，「ストレス」，「憂鬱」などの感情とも結びついているとされる。

「生命感覚」は，自分の身体内にあるこの感覚が，「痛み，欲求，快感，不快」を引き起こす。レーバーは，「生命感覚」によって身体に引き起こされた感覚内容が，固有な「感情」をも作り出すという。

> 嫉妬，勝気，自負，思い上がり，怒り，喜びのような感情，しかしまたまったく対極にある節度，慎みのような感情もまた，生命感覚の中で身体と結びついた根源をもつ［略］。（ebd. 124）

体内にあるとされる「生命感覚」によって引用文に示されているような感情が引き起こされる。レーバーは，これらの感情が，人間生活のための基礎，基盤を形成するのだという。

「運動感覚」は，自己の動きを知覚するものであり，空間における自己の身体性の感覚を伝達し，自己の諸行為，身振り，意志表示を自身で体験可能，知覚可能にする。このように「運動感覚」は，自己が移動するという感覚である。また自己の動きと外界との対照によって，外的存在物に「時間」という特徴が加えられる。また，自身の動きに関しては，自己のそれぞれの行為の適切な速さを体得することもこの感覚の機能であるという（ebd.）。

ここで，「運動感覚」と「意志」との関連も語られる。

> 意志の表明，あることに向けられる努力，創造意欲，人間的絆の欲求，より高いねらい，より卓越した内容がある目標を追い求める普遍的な切望，心構えは，［略］この感覚域に分類することができる。（ebd.）

上のような意志に基づく精神活動が貫徹される場合には，プラスの感情が生まれるが，そうでない場合には，「不安，抑制，自信のなさ」（ebd. 125）の感情を引き起こす。

「平衡感覚」は，空間的位置感覚と関係し，なかんずく直立と関係する。この感覚は，中央の位置，まっすぐ，平ら，等しさと関係し，中央からのずれ，傾き，ゆがみ，不釣り合いを知覚する。次のような感情をもたらす。

> 直立のエネルギーは，体重を克服し，対立や隔たりのための感情をもたらし，自己の存在に対する嫌悪や感覚内容をも強化する。だが婉曲的に，心配，底知れなさ，気味悪さ，不気味さもまた引き起こしうる。（ebd. 125f.）

「平衡感覚は」，調和の感覚であり，釣り合いが保たれているか，均一であるかどうかを体験する感覚である。

> バランスの良い状態を感じている魂は，落ち着きを可能にする。温厚，「庇護されているという感情」は，このような感覚の経験がないとしたら決して説明がつかない。（ebd. 126）

レーバーの「平衡感覚」と関係する感情の説明は，以上であるが，彼はさらに，この感覚と人間認識（「思考」）との関係を指摘する。この感覚グループが関係するのは，感情だけではないとしながら，彼は次のように続ける。

> 身体感覚とそれによって伝達される体験の質は，高次の認識過程にも多様に関与している。これらの感覚は，きわめて無自覚的にではあるが，それだけ一層魂を束縛する。幾何学，算術，数学の認識において，そして論理学において，正しさ，整合性，アプリオリな理解可能性の基礎的感情を伝える働きをする。（ebd.）

「平衡感覚」（及び「運動感覚」）が数学的認識の土台であることは，シュタイナーが指摘していることである（zwölf. 25）。この点においても，レーバーはシュタイナーの論を忠実に継承している。

⑵ 「感情感覚」に基づく感情

レーバーは，この感覚グループを「世界感覚」と呼ぶのだが，これらの感覚が「一方において，生体を世界の中にある物質性と関係づけ，他方において人間を取り囲む周辺全体と関係づける」からだという（Menschenkunde 126）。

「嗅覚」は，世界の物質の表面的なものと人間をつなげ，人間内面の奥深くに触れる。匂いや香りは，感情の手近に

あり，感性体験に直接作用する。どのようにか。「元気づけ，感覚を麻痺させ，心地よくさせ，不快にさせ，感傷的にさせ，吐気をもようさせる」（ebd.）。

物質が発する匂いを嗅ぐことによって，上のような感情が直接引き起こされる。「嗅覚」はこのように，外部感覚であると同時に，内部感覚でもある。

「味覚」は，物質それ自体の中に入り込む，「化学的感覚 der chemische Sinnそのもの」（ebd. 127）と表現されている。レーバーの記述において「味覚」により生じる感情については言葉少なである。むしろその精神との関係が指摘されている。「味覚は，芸術感情，美学の全領域に存在する。味覚の知覚内容は，何よりも精神生活全体に作用する」（ebd.）。

「味覚」は，五感の一つとして一般的に馴染みのものである。レーバーの説明は，「味覚」が他の感覚と協同することで，「意識下」において精神に作用する感覚であることに注意を向ける。

「視覚」に関しては，シュタイナー同様に，ゲーテ（Johann Wolfgang von Goethe）の色彩論が前提にされている。ゲーテの研究成果である「色彩の感覚的精神的作用」がそのまま引用，紹介されている。以下は，ゲーテの「色彩論」からの引用である。

> プラスの側の色彩は，黄色，赤黄色（橙色），黄赤色（朱色）である。これらの色彩は，活発で，生気に満ちた，努力を誘う気分にさせる。／［略］マイナスの側の色彩は，青，赤青色，青赤色である。これらの色彩は，不安な，柔和な，憧憬的感情にする。（ebd.）（Goethe 495,497）

レーバーは，ゲーテの色彩論からの引用に続いて，「ゲーテの言葉から，光と色彩の知覚内容は，深い感情を刺激しうることが示唆される」（Menschenkunde 127）と書いている。つまり「視覚」は，深い感情を引き起こすというのである。

「熱感覚」は，体全体に空間的に浸透する性質をもっている。「熱感覚」は，「生命感覚」と密接な関係がある（ebd.）。その意味で「熱感覚」は，外部刺激によって，内面に無意識的な作用を生じさせる。レーバーは，この感覚の感情への作用について次のように書いている。

> 熱感覚は，人の心を冷たくしたり，暖かくしたりしうる。しかし冷や汗もまた生じさせうる。熱感覚に続いて，感情としての心の温かさや感情の冷たさが生じる。適温なのに，心をぞくぞくさせることもありうる。温かな感情は誰にでもわかり，人情味や感情の激しさもわかる。（ebd. 127f.）

「熱感覚」は，引用文にあるように，外的物質の刺激だけでなく，人からも刺激を受け，その結果，内面に上のような感情を生じさせる。

レーバーは，このグループの４つの感覚に共通する特徴について次のように書いている。

> この感覚グループは，強く直接的に感情に作用する。これらの感覚によって引き起こされる感情は，一方において感覚的刺激に依存し，他方において［略］生命の基盤状態へと作用しうる，しかも満足や快適，嫌悪感と不快感といった両極的な方向へ。（ebd. 128）

これらの感覚グループによる知覚内容は，感情に作用すると同時に，生体内に無意識下にも作用するという。さらにレーバーは，直接的な刺激を受けて生じた上のような感情が，しだいに「賛美，尊敬，美的感情」といった「認識感覚」に発展するものであることを指摘している。

⑶ 「認識感覚」に基づく感情

「認識感覚」は，外部刺激を自覚的に受容する感覚である。レーバーは，この感覚グループを「精神的時間的事象を把握するための感覚」（ebd.）と表現している。この感覚グループに関して，一般的に「聴覚」しか知られていない。「言語感覚」，「思考感覚」，「自我感覚」は，シュタイナーによって見出されたものであるとされる。

「聴覚」に関するレーバーの説明は，シュタイナーと少し異なっている。シュタイナーは，「音感覚，響き感覚と，他方で言葉感覚Wortesinnとを区別すべきことに気づかなければなりません。」（zwölf 10）としている。シュタイナーの場合，「聴覚」と「言語感覚」との違いに注意が向けられている。それに対してレーバーは，「聴覚」と「音感覚，響き感覚」を区別している。そして「言語感覚」と「思考感覚」を同列に扱っているように思われる。

レーバーはいう，「音あるいは響き感覚は，聴覚と密接に結びついているのだが，独自の感覚として聴覚と区別される」（Menschenkunde 128）と。そして「聴覚」は，物の内容物の特性と均整の程度を知覚する器官であり，すべての物体には，音が内在しているというのである。例で語られている音は，音楽と人間の声である。

> 人間の声は，外部に対する内面性の告白である。［略］音の世界は，心に語りかける。人間は，音楽の中で，心のメッセージの中で理解し合う。情感の深み，集中，感動は，音の世界によって呼び覚まされる。（ebd. 128）

これに対して「音あるいは響き感覚」は，音の要素を聴き分けることが問題になっている。音楽の場合は，「音程」「色調」「和音」「不協和音」を聴き分ける。そして音声の場合は，音節を聴き分けることが問題となる。「音節は母音によって音色をつけられる。OとUはより低く，EとIはより高く，Aはその中間にある。このような音の性質が魂の声を呼び覚ますのは明らかである。逆に音の性質が魂の声を表現できることも自明である。uによってぞっとすること，aによってびっくりすること，ehによって反感を覚えること，i-gittによって嫌悪が表現される」（ebd. 129）。

このようにレーバーは,「聴覚」と「音あるいは響き感覚」を区別している。

これに対して「言語感覚」と「思考感覚」については,両者を同列に並べ次のように書いている。

> 思考感覚と言語感覚は，内面的な知覚内容を通して，言葉の意味と，語られる言語の思考内容を直接捉えさせる。言葉を聞く際に，言葉の内容と意味が，思考の共体験と表象によって直接把握されることにより，その中に固有の感覚が働いていることが明らかになる。(ebd.)

「内面的な知覚内容を通して」とは,「思考感覚」「言語感覚」のような「認識感覚」は,「感情感覚」や「意志感覚」と連動することによって初めて機能することを意味している。この両感覚によって引き起こされる感情は,「疑惑,不信,疑問,優柔不断,慎重な吟味」(ebd. 130)である。レーバーの記述にはないが，これらの対極にある感情，例えば確信，信頼なども，この感覚によって引き起こされるものと考えられる。

「自我感覚」は,既にシュタイナーの説明にあったように,他者の自我を知覚する感覚である。(註4)「自我感覚」によって生じる感情は，レーバーによれば,「親密さ，魅力」などである一方で,「馴染みなさ，拒絶，無理解，疎外，距離感」なども入るという（ebd. 130f.)。

以上３グループの感覚が，それぞれ独自に，また相互に関わり合って，どのような感情を引き起こすかについてみてきた。レーバーは，感情と感覚について次のように書いている。

> 感情は，感覚と結びつくことによって，感覚の働きそのものを通して秩序を受け取る。このことは，自我知覚内容が示すように，よりはっきりしない欲求や衝動と完全な対照をなすが，情熱のパッと燃え上がる激情，相応のかき立てる気分とも対照をなす。なぜなら＜感情の秩序＞は，感覚の機能によって構造化され，それによって感情は，ある種の組織を獲得し，＜抑制される＞からである。(ebd. 131)

感情と感覚とは，密接な関係がある。各感覚は，それぞれに対応した感情を引き起こす。さらに，感覚の伸長は,大人のあるべき感情の成長へとつながる。ヴァルドルフ教育では，３グループの感覚が，主に発達する時期があること，そして成長に応じて，感覚と関わりながら，感情等も変わっていくものであると捉えられている。

4　S.レーバーの「12感覚」解説 (2)
―発達時期の観点から―

「12感覚」は，全体で有機的統一体を形成するが，既にみた３分類の感覚グループには，それぞれとくに発達の盛んな時期がある。レーバーは，先にみたシュタイナーによる分類に従いながら，３グループの「12感覚」と，発達時期との関係について解説する。ヴァルドルフ教育における発達観は,「12感覚」と密接な関係があることが示される。本節は，レーバーの著書の第三部「青少年時代」からのものである。

(1)　第１七年期と「12感覚」

「第１七年期」は，ヴァルドルフ教育においては，誕生から歯が生えかわる７才ごろまでの期間である。この時期における諸感覚の発達について，レーバーの記述を，拾うことにしよう。

> 最初の幼少期に発達の大きな原動力があるのは，身体感覚―触覚，生命感覚，運動感覚，平衡感覚―である。新生児は,成人よりもはるかに内容豊かに皮膚の接触(触覚）を感じる。これによって安心感，温かさ，生活感情,生存に関わる確信が広がり,幼児に信頼感を与える。[略]この経過において，身体の状態を知覚する生命感覚がともに作用する。(ebd. 432)

誕生以後の幼少時期は「身体感覚」が活発になる。引用文で注目すべきは,「触覚」,「生命感覚」に関する記述である。新生児，乳児における「触覚」の特性，この感覚に対する周囲の大人のかかわり方が,「生命感覚」をも介して,人間最初の時期において，人間精神の成長の基礎形成の核になる。ヴァルドルフ教育においては,乳幼児期の「触覚」に対する刺激は十分な配慮が必要であるとされる。

レーバーによれば，並び順では聴覚から始まる「認識感覚」もまた，早い時期に発達する。

> １年後には，言語感覚が明確に発達する。幼児は，自分で話すことがなくても聞き取ることができる。活発な言語能力を獲得すると，自分自身の思考の働きに気づくことができる。[略] ３才の幼児は，他人の思考の知覚に目覚める。これに対して他人の自我の知覚は，もっとずっと早く，８カ月と18カ月との間である。「人見知り」が始まると，自我感覚は確かなものとなる。(ebd. 432f.)

人は，言葉の分からない状態で誕生し，しだいに言葉を獲得していく。どのようにか。レーバーは,「言語感覚」により意味が分からずとも，受動的な受け取りから始まり,まずは物音と言葉の違いが分かるようになるという。したがって,「聴覚」と「言語感覚」の異なる二つの感覚を想定しなければならない。言葉のやり取りが活発になると，自分が思考していることに気づくようになる。それに伴って，他者の思考にも気づくようになる。これらはいずれも直観的なレベルで行われる。「人見知り」は，身近な大人の自我と未知の人との自我の知覚の違いを感じ分けることである。それは,「自我感覚」の働きによるものである。さらに乳幼児は,「自我感覚」をもつために，つまり他者の「自我」を知覚できるために，この時期の身近な大人の

関わり方によって，その身体と精神に大きな影響を及ぼすとされる（ebd. 433）。

レーバーは，３グループの関係性の視点から，この時期の特徴を次のように説明している。

> 知覚内容，知覚対象によって強く影響を受けるので，中位と上位の感覚は，下位の感覚から切り離されて現われることはない。自分の生命過程との統一的関係が常に決定的に影響する。すなわちすべての知覚内容は，生命プロセスに直接影響する。（ebd. 436）

乳幼児の期間は，「身体感覚」が主に発達することを既にみた。これらの感覚によって受容される感覚内容は，「生命過程」の基礎となるものであり，それゆえ「思考感覚」グループと「感情感覚」グループも同時に影響を受ける。レーバーは，幼児期に特徴的な「自己中心性」は，後者２つのグループがまだ十分に独立していなく，「身体感覚」と一体化しているために起きる現象であると解説する。ヴァルドルフ教育における，「幼児は感覚器官そのもの」という表現は，「12感覚」論に根ざしたものである。

⑵　第２七年期

「第２七年期」は，ヴァルドルフ教育では７才頃から性的成熟に至る頃までの期間である。この時期は，学齢期頃から始まる。レーバーによれば，この時期になると「感情感覚」の働きが活発に伸長する。そして，これらの諸感覚と，「認識感覚」及び「意志感覚」とが，幼児期とは異なる結びつき方をする。「意志感覚」との結びつきの例を，レーバーは次のように書いている。

> 今や強化された個々の感覚の発達によって，優勢な中位の諸感覚と結びつく形で，下位の諸感覚さえも遡及して変化する。それが特徴的に見られるのは，まさに子ども時代の中期において例えば，一方では，平衡感覚（幾何学）や運動感覚（算術）と非常に強く結びついている数学的な能力が際立ってくることである。これらの能力の基礎にある力は，この場合，自己の身体の知覚内容に役立つのではなく，外的世界の諸構造や諸関係の把握のために役立つ。（ebd. 436f.）

ヴァルドルフ学校における算数の授業方法の一つの原理が，「12感覚」論に源泉があることがわかる。「平衡感覚」「運動感覚」は，下位感覚グループ「身体感覚」に属するものであり，もともと自分の内面状態を知覚する感覚グループである。だが「数学的な能力」が問題になる場合は，下位感覚グループと「認識感覚」グループとの連携が必要であるという。つまり「身体感覚」が幾何学や算術と結びつくと捉えられている。このため数学的能力を発揮するためには，「平衡感覚」と「運動感覚」が乳幼児期おいて十分に発達している必要がある。レーバーは，「歯牙交代までに内面において働いたものによって外的世界を把握する」（GA 322）[註５]というシュタイナーの感覚論を引用している。

レーバーは，「感情感覚」グループが「第２七年期」において優勢になり，次のような場合に現われる，と続ける。

> ［略］「触覚と運動感覚による知覚内容」が，距離感覚であるところの目と耳によって抑制される。同時に目と耳は，（高まる表象力と並んで）その能力を高める。７才と14才の間での明度の区別は倍加し，色の区別の繊細さが同期において90％を下回らない程度に発達する。10才児の音の高さの識別力は，６才児の５倍である。（ebd. 437）

この時期において，距離感に関して，第３グループの「触覚」と「運動感覚」を，第２グループの「視覚」と第１グループの「聴覚」の感覚機能の方が圧倒するという。同時に「視覚」「聴覚」は，同時期に高まる表象力と一緒になり，その能力を高めるという。つまり，この時期は，主に第２グループが活発に働くが，その他のグループとの関係性の視点も重要であるというのである。

⑶　第３七年期

「第３七年期」は，ヴァルドルフ教育では性的成熟以降の７年間である。この期間は，上位の感覚グループ「認識感覚」が最も発達する時期である。前の２期と同様に，この時期の感覚も，周りの世界についての諸性質の知覚内容を，直接，すなわち思考を介在させることなく知覚する。

> ［略］関心が，基本的に音楽に向けられる。聴覚を通して，14才と17才との間に，音の高さの違いの感度が増す。その際音楽との関わりは，［略］このような感度を著しく高めうる。／音楽性の幅広い多様な世界が，完全に開かれる。（ebd. 437f.）

前２期における「聴覚」は，主に音を聴き分ける機能をしていた。この時期の「聴覚」は，さらなる発達を遂げ，音の味わい，音楽の多様な世界を受容するようになるという。もちろん，「音楽性」の開花は，「聴覚」が主要な働きをするが，他の感覚との共同作業で可能となる。

「言語感覚」はどうか。

> 言語能力の世界は，多岐にわたって変化を遂げる。思春期前期から始まる青少年期において盛んに読書が行われ，語られ―沈黙もあるのだが―朗読される。詩が見出され，抒情詩が味わわれるだけでなく，内面に苦悩が満ちる場合でもいやそれだからこそ，しばしば自作される。（ebd. 438f.）

引用文において，一般に捉えられるこの時期の言語力と，いわゆる「言語感覚」力との違いを見出すことはできない。上でみたこの時期の「聴覚」と同じようなことがいえるかもしれない。この時期の「言語感覚」は，言葉の聞き取り

の段階からさらに進んで，言葉の背後にあるものも知覚できるようになる。

「認識感覚」グループにある「思考感覚」と「自我感覚」に関しても上の２つの感覚と同様に，認識力と感覚とが，明確に分けて論じられているわけではない。「言語感覚」に続いて「思考感覚」について，次のようにある。

> 同じことは，思考感覚が関係する，さらに高まる議論についてもいえる。思春期それ自体というよりも，青年期において，思考組織がデザインされ，［略］世界観全体が形成される。［略］（他者の考えを―土屋）追体験しながら，自分の思考，認識獲得の努力が行われ，自分の判断が訓練される。（ebd. 439）

引用文では，この時期に始まりしだいに盛んになっていく他者との議論の場において，「思考感覚」が働くと書かれている。ここでは，議論の際に機能する感覚としての「思考感覚」の受容内容と，思考活動との関係についての記述はみられない。

「自我感覚」についてはどうか。

> 同様の努力は，親しい相手Duをめぐっても顕著になる。重要なのは，抽象的な見解，哲学的学説，尊敬概念，倫理学ではなく，それらを具現化する人間達であり，その際作用する彼らの自我である。［略］彼らが重要になり，意味をもつようになるのは，自我感覚，すなわち他者の知覚内容が働こうとするからである。（ebd.）

思春期以降における「自我感覚」の役割は，抽象的，観念的な思想などを具現化する他者の自我を知覚することである。「自我感覚」の対象は，一般的，抽象的なものではなく，目の前にいる具体的な人間の自我を知覚することである。つまり，この時期において，理論や観念だけが重要なのではなく，目の前にいる生身の人間を直観的に見抜くことも必要であることが説かれている。ここにおいても，「思考感覚」と同じように，「自我感覚」が他者の自我を知覚する際に機能するとされているが，知覚結果が，自らの自我にどのように作用するかは触れられていない。

レーバーは，「認識感覚」グループの機能は，この時期において高まるという。

> ［略］上位感覚は，思春期において［略］自立性が高くなる。この感覚グループにおいては，概念や表象に依存することなく，その知覚内容が，自覚的に意識に直接伝わる。（ebd.）

引用文のように，「自我感覚」は，具体的に目の前にいる身近な人間の自我を知覚する感覚である。「自我感覚」は，思春期以降に他の諸感覚と連動しながら，大きく発達するとされる。(註6)

5　まとめと課題

本稿は，シュタイナーの「12感覚」がヴァルドルフ教育においてどのように論じられているかに焦点をあてた。これらの検討から得られた知見は以下である。

第一に，シュタイナーの「12感覚」は，ヴァルドルフ教育の中に継承されていることが確認された。

第二に，「12感覚」論は，人間を一つの統一的有機体として捉えるべきことを提起している。「12感覚」は，「表象」「感情」「意志」と関係しながら，それぞれ独立したものではなく，相互に関わり合いながら機能するものと考えられている。例えば，乳幼児の「自我感覚」「思考感覚」は，それだけで機能するのではなく，「意志感覚」に分類されている「平衡感覚」「運動感覚」「生命感覚」「触覚」と協同することによって，感覚内容が真に取得される。「自我感覚」と「思考感覚」等は，他者の人間性や考え方等を知覚する感覚である。これらの外部感覚が得た内容に対応する内部感覚の機能が想定されている。自覚的な感覚と，無自覚的な感覚の結びつきの数多くの体験を繰り返しながら，乳幼児なりの，周りの人間等に対する感覚的認識が成立すると考えられている。心理学的にいえば，内部感覚を想定することによって，ある意味で無意識の心理機能を可視化している。

第三に，「12感覚」は，望ましい人間発達のあり方の一つの側面を想定している。各感覚グループ，諸感覚の発達は，それぞれ優勢な時期がありながら，相互に密接に関係する。ヴァルドルフ教育における最初の７年間は，「内部感覚」の発達が優勢な時期である。これらの感覚の発達が，次の時期の発達のために不可欠と考えられている。一方，「認識感覚」の「自我感覚」「思考感覚」「言語感覚」等は，この時期は「内部感覚」よりも発達は緩やかである。しかし，緩やかであることが価値の低さを意味するものではない。この時期に発達した「認識感覚」は，第２七年期を経ながら得られた感覚内容を確かな基盤にして，第３七年期に，飛躍的発達をすると考えられている。

第四に，「12感覚」は，ヴァルドルフ学校において，教育の方向づけを示しうる。現代諸科学，例えば，脳科学，神経心理学，身体心理学など，人間の思考や身体，感覚器官についての学問は進展を遂げている。これら現代の諸科学からみれば，シュタイナーの「12感覚」は，科学以前の一つのアイディアという評価を受けるかもしれない。しかし，現代諸科学の成果が学校教育に直接に反映されるとは必ずしもいえない。シュタイナーの「12感覚」は，いわば「基本原理」の一つなのであり，それに即した教育が目指されているという点で，ヴァルドルフ学校の教育方針にブレは生じない。

残された課題は，思考と「思考感覚」との違い，「自我」と「自我感覚」との関係性などを更に検討することである。これにより，「12感覚」の特徴及びその教育に果たす役割も，より明確になるはずである。

＜註＞

(1) 日本における「12感覚」の先行研究は，高橋巖を挙げることができる(参考文献等を参照のこと)。高橋の当該研究は，シュタイナー「霊学」の範疇での論考が中心である。「12感覚」に関する文献には，例えば，オランダの医師アルバート･ズスマン（Albert Soesman）の『12感覚』がある。彼は医師であり，医学に立脚しながら，シュタイナーが提唱する「12感覚」を解説している。この本は，医学的見地からの「12感覚」の記述も多くみられるが，一貫してシュタイナー「霊学」を基本的視点にしている。ヴァルドルフ教育関係者以外の者にとって，必ずしも解りやすいテキストとはいえない。参考文献(3)。

(2) 「12感覚」のまとまった唯一のテキストは，『魂の謎について』の本文の註のための補遺，「志向的関係の真の基礎」である。(**rätseln** 143-149)

(3) 12の感覚器官の３グループと，「認識」「感情」「意志」との関係性について，『教育の基礎としての一般人間学』の第８講で，シュタイナーは比較的詳しく説明している。そこでは，12感覚の多様な組み合わせが，「判断」等を生むこと，12感覚と「認識」「感情」「意志」とが相互に密接に関連していること等が語られている。参考文献(6)と(7)を参照のこと。

(4) 人間の「自我」についてレーバーは，シェリングとフィヒテを援用しながら，次のように短く触れている。「自己が知覚経験をする自我は，自我の原型としての同一性に根ざしている。自我は内容それ自体ではなく，主体ではなく，同定の行為そのものである」(Menschenkunde 130)。

(5) シュタイナー全集322巻『自然認識の限界』

(6) レーバーは，この章の最後に感覚プロセスは，認識事象の要因の一つに過ぎないと断り，「表象形成」と「判断形成」について考察したいと書いている（Menschenkunde 440)。そしてこれらについて後ろの章で論じている。これらの論の検討は，本稿の課題として残る。

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新学習指導要領に見るコミュニケーション重視の英語授業観

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An Inquiry into Communication-oriented English Teaching and Learning at Schools

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Abstract

This paper gives an overview of the goals of English teaching and learning in regards to proposed guidelines in the New Course of Study - Foreign Language & English, which is to be introduced in 2020. Additionally, this paper suggests ways which facilitate self-directed learning which takes into account the students' academic abilities. This includes three components; knowledge, attitudes and skills. Since the Heisei era, there have been gradual changes in English educational policies for cultivating global citizenship. This has seen a shift from teacher-led instruction to learner-centered communicative approaches. Although the concept of "communicative competence" has been considered an essential quality for English learners, it seems that teachers of English and educationalists have yet to reach a consensus on what this requires. In the Post-Method Era, it is difficult to determine which strategies are the most appropriate for individual learners. The methodologies that teachers adopt, and indirect learning strategies that learners employ, will be more critical than ever. As accommodators, teachers will be required to provide students with learning strategies that help them to undertake effective learning. To be lifelong learners, or successful communicators, students need to develop self-directed learning skills. At the same time they need to be flexible as the need requires. This goal can be attained through a wide range of learning experiences. [1)]

Key words: 新しい学力概念、コミュニケーション重視の授業

1　問題の所在

中学校・高等学校の学習指導要領（外国語）で英語教育の目的が初めて「コミュニケーション」と明記されてからおよそ30年が経過した。1989年の改訂から４技能を統合したコミュニケーション能力の育成が明文化され，2013年度施行の高等学校指導要領では，指導形態として文法指導を言語活動と一体となって行うこと，英語の授業は原則英語で行うことなどの文言が掲げられた。[2)] その根底には，問題解決型の学力を重視した新しい教育への転換がある。この学力概念は2020年以降に順次予定されている学習指導要領の改訂に向けて，いわゆる21世紀型学力として確実にその地歩を固めている。本稿では，平成に入ってからの英語教育の現場を振り返り，指導者側の立場から今後の英語教育の現場で取り組むべき課題について検討する。

平成元年から文部省（現・文部科学省）は，グローバル化する社会に対応する力として，主体的に学ぶ態度や思考力や表現力の育成を重視する学力観をめざしてきた。これはその後も数回にわたる学習指導要領の改訂を経て堅持され，『生きる力』の育成を確固たる狙いとして定着しつつある。[3)] この学力概念では，⑴基本的な知識･技能，⑵知識･技能を活用した課題解決能力，⑶学習意欲，が主要な３要素と規定されている。教師は，教科指導を通して生徒の自発的な社会参画および社会形成者としての力を育むことが求められる。生徒にとっては，学習内容の習得とともに学ぶ姿勢に基づく学習プロセスそのものが評価される。この動きは，中等教育の現場でもアクティブラーニングという学習スタイルとして浸透しているが，今後これはさらに推奨され，より積極的に行われることになる。常に変化する社会の中で，獲得した知識をどのように活用できるかを探究するのは，学校教育全体の共通課題となっている。こうした流れに目を向けつつ，英語教育の現場において百家争鳴の議論を呼び込んだコミュニケーション重視の授業観を，ここで今一度見つめ直すことは無意味なことではないと考える。

平成29年７月７日受理

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2　コミュニケーション重視の学力観とは

外国語教育の要諦である「積極的にコミュニケーションを図る態度」も，前述の教育理念の実現に向けた学習の方向性を言い表したものである。社会言語学者の鈴木孝夫氏（1999）は，「相手を理解して，できる限り相手のようになる…完全に内向きで，自己改造型の外国語教育」が長い間行われてきたことを批判していた。氏は国際理解の名のもとに自発性とは無関係な学習内容を暗記するだけの非能率的な英語教育を改善し，身近な環境を能動的に表現してこそ必要な英語力が身につくのだと主張する。[4)] 1980年以前の中学検定教科書では英米の題材が中心であり，英語母語話者を絶対的なモデルとして学ぶことがいわば暗黙の前

提であった。その後，文化交流が相互性を持つという反省から，英米中心の地域語としての英語から他者との共生を可能にする国際共通語としての英語習得に重点がシフトした。1969年以降の学習指導要領の変遷を見ると，この理念は基本的に引き継がれて敷衍した言説となっている。日本学術会議「大学分野別質保証の在り方について一回答」（2010年７月）では，コミュニケーションは「…自らとは異なる意見，感覚を持つ人々と出会い，それを『聴く』能力こそが重要であり，その上で対話が可能になるのである。対話とは，それを通じて自らの意見や感覚が変容する可能性を秘めた営みであり，他者との出会い，違和感の経験こそが対話の出発点である」と明記されている。ここで「聴く」能力とは他者を理解しようとする姿勢であり，コミュニケーションとは相互理解を目的とした「対話」の実践であると説く。

平成の英語教育の変革は，他文化を一方的に受容する姿勢を改め，相互理解に向けた分かりやすさに重点を置く発信型の学習活動へ転換することであった。高度で完璧な英語を追求する中で，ともすれば言語能力の不足とみなされるかもしれない言語使用上の誤りは，言語行為中心のアプローチでは役に立つ有意義な言語活動とみなされ，意思疎通が遂行されれば成功と認められる（長谷川2013）。つまりコミュニケーション重視の英語教育では言語形式の正確な使用や流暢さが必ずしも優先されるわけではなく，目標言語を通じて様々な課題に取り組む姿勢や意欲そのものが評価の対象となる。その意味において，英語で授業を行うことは，教師と生徒が目標言語の使用に伴う違和感あるいは理解不能性に向き合う「対話」を実践する機会になりうる。究極的には必要な英語力の習得を前提としながらも，目標言語による言語活動を通じて社会の諸状況に対応できる異文化理解力を育むことが意図されている。このような対話重視の教育では単なる技能を超えて，指導者と学習者双方の人格的な関わりが指導の根幹を成す。

こうした流れを受けて，英語教育の学校現場でも，生徒主体の活発でユニークな授業が行われるようになってきている。その一方で，コミュニケーションという用語について教育現場での認識の相違がみられる。入学受験や資格取得といった道具的動機付けの面が英語学習に強く反映され，学んだ事柄を記憶・再生するという学習観がまだ根強い。もちろん，それは重要な学習スタイルの一つには違いないが，ペーパーテストで高得点を取るのはほんの一側面の学力にすぎない。また依然として英語圏の文化に対する漠然とした憧れが英語に対する日本人の統合的動機付けを支えている面があり，教育現場での目標設定に関して一定のコンセンサスが得られていないのが現状であろう。自らの生活状況を自発的に英語で発信するという指導や学習に繋げていくには，公教育において取り組むべき課題は多くある。[5)] いずれ新学習指導要領では，生徒個人に対して断片的な知識伝授を積み重ねていく方法が見直され，他者との交流を通して行う協働学習の面が重視される。そして今後，学校現場では「知識の記憶→練習→再生」という伝統的な学習プロセスに対比すべきものとして，「知識の理解→協働的創造→発信」の流れが確立した共通認識としてますます実践されていくことになる。

3　英語教育において求められるコミュニケーション能力

そもそも英語によるコミュニケーションとはどのような事態をいうのだろうか。仮に英語による意思疎通が正常に遂行されている事態をいうのであれば，それを可能にしているものは何か。はじめに，よく知られたCanale&Swain（1980）が定義するコミュニケーションに必要な要素を確認する。

⑴　文法能力（Grammatical Competence）　語彙，文法を駆使して文を作れる能力。
⑵　談話能力（Discourse Competence）　文をつなげて会話ができる能力。
⑶　方略能力（Strategic Competence）　コミュニケーションを円滑に進めることができる能力。
⑷　社会言語能力（Sociolinguistic Competence）　社会的な規則に従って適切に言語を使える能力。

コミュニケーション能力の定義（Canale & Swain, 1980）

まず，⑴の段階では音声体系，単語，文法を知っており，一文であれば正しい文を作ることができる。しかし，文自体が正しくても，対話の中で自然な文を産出できなければ，談話能力を欠いているということになる。文法規則に従いうまく単語を組み合わせて文を作れたつもりでも，どこか不自然な文になってしまうことがある。これは文法規則を知っているだけでは不完全な伝達になる場合があることを意味する。社会言語能力は，状況や相手によって適切な表現を駆使できる力である。例えば，目上の人に対して“Will you ~ ?”のような表現を使うことができず，“Could you ~ ?”や“Would you mind ~ ?”を使わなければならないなど，当該文化圏の習慣にふさわしい表現を使うことが求められる。さらに，コミュニケーション上で何か問題があった場合，それに対処したり修正できる能力が方略能力である。

但し，⑴〜⑷の分類は言語能力のみに焦点をあてたものである。90年代になると，ことば以外の要素を中心にコミュニケーションを広く捉え直す動きがでてきた。その一例として，Byram（1997）が提示した異文化理解能力モデル（Intercultural Communicative Competence）がある。このモデルでは，必要な異文化理解能力として以下の３要素が関連している。

⑴　態度（attitude）
　好奇心と寛容性。他文化への誤った見方や自文化への見方を保留する姿勢。
⑵　知識（knowledge）

自らが所属する集団と他者が所属する集団の慣習についての知識。

社会レベル及び個人レベルでインタラクトできるプロセスに関する知識。

⑶　技能（skill）

①　解釈できる能力

他文化の事象や文書を解釈し，それを説明でき，自文化の文書と関連付けられる能力。

②　発見できる能力

ある文化とその習慣についての新たな知識を獲得する能力。リアルタイムのコミュニケーションとインタラクションという制約のもとで知識，態度，技能を活用する能力。

異文化理解能力のモデル（Byram, 2007）

異文化理解という用語は世間でも広く使われているが，単に外国文化との交流を通じてその認識を深めるというだけではない。ここでは他文化を通じて自文化を見つめ直そうという視点も含まれている。ここでの“skill”とは，得た知識を様々な事象と関連させて活用しようとする姿勢につなげ，そこからまた新たな知識を得るという不断の学習プロセスに他ならない。これは「主体的な学び」を主眼とする新しい学力観にそのまま重なるものであると言えよう。様々な次元が想定されるコミュニケーションという用語を一義的に言い表すのは困難であるが，90年以降，記憶再生型から問題解決型へ中心課題がシフトするのとほぼ機を同じくして，コミュニケーション能力が言語運用能力にとどまらず，学習者の人格や生き方そのものに関わる問題として捉えられるようになった点は注目に値する。なおこのモデルは，ヨーロッパ共通参照枠CEFL（Common European Framework of Reference for Language）（2001）の設定にも貢献しており，竹内（2012）によれば，その妥当性を検証する研究も複数存在する。

2008年12月に学習指導要領改訂案が公表されたとき，改訂意図をめぐる賛否両論が巻き起こった。改訂趣旨としては「４技能を統合的に活用できるコミュニケーション能力の育成」であり，その中核となる文法はコミュニケーションを支えるものとしてとらえ，言語活動と一体的に行うというものである。高等学校の授業では，実際の言語活動の現場とするためにできるだけ多くの英語に触れ，得た知識を自分のものとして咀嚼し，ディスカッションやプレゼンテーションといった様々な活動を通して表現することが求められる。さらに，英語による指導を基本にその目的が達成されなければならないとしている。こうした指導法は2021年度から中学校でも完全実践される予定となっている。バイリンガル教育について論じられる際，よく引き合いに出されるCummins（1979）の区分概念で言えば，読み書きや論理的思考・分析力を含めた認知学習言語能力（CALP）の育成を視野に入れた指導が前提となろう。この改定案が公表された当初，特に英語で授業を行うことについて，「可能であるのか」，「効果があるのか」といった論点で，学校現場や教育関係者の間で論争が繰り広げられた。しかし，コミュニケーションをスキルの問題に矮小化した言説が流布したため，「教養か実用か」，「文法中心か音声中心か」，「読み書きよりも会話重視か」といった単純な二項対立で捉えられ，指導目的よりも指導方法に焦点を置く議論が多く生じることとなった。現場に少なからぬ混乱を招いたのは，個人の指導観が入り乱れて目的と具体的指導方法の両輪で合意を形成できなかった部分が大きいと思われる。[6)]

従来型からコミュニケーション重視の授業への転換には，和訳や文法解説のみに終始しがちな授業への反省もあるが，世界規模で推進されている問題解決型の学習観への転換が底流にある。[7)] これに伴い，学習効率をどのように向上させるかという実践面での課題はあるものの，まずは自発的な学習を誘発しようという指導観への切り替えが重要であったものと思われる。改訂趣旨は従来の言語形式に偏重する教育を見直し，これまで教師主導だった授業を生徒が主体となって行うことである。そのための環境づくりとして，英語の授業は広範囲な学習内容を扱った言語活動を中心に行うことである。グローバル社会では，絶えず社会が変化していて，個人を取り巻く生活状況も様々な様相を見せる。従って，知識は固定されたものではなく，社会の変化に応じて改変され更新されなければならない。問題解決能力が学力育成のための世界的な基準となっている中で，目標言語の自律的獲得のプロセスを「体験する」ことが，知識を積み重ねていくような，ともすれば受動的になりがちな従来型の学習観に優先する。英語で授業を行うことはこうした態度を重視する指導方略の一つであり，機械的模倣と反復練習による言語獲得を狙いとしたかつてのオーディオリンガル・メソッド（audiolingual method）とは本質的に異なる。英会話自体が目的化してしまうことがあってはならないのは言うまでもない。そして新しい学力観では，人格陶冶も含めた広い意味での英語力向上が目指すべき到達点となる。学習方法としてのスキルの問題ではなく，言語能力と人格形成を一体化させたコミュニケーション能力の育成を通して英語力を育てていく。現存の学習内容の重要性を踏まえつつ，多層的な（教師と生徒，生徒と学習内容，母語と目標言語，生徒間の）対話を基盤とした学びの質への転換が求められているのだと言えよう。

4　学校現場の現状と課題

ここまで，今後求められる新しい学力の概念を踏まえて，コミュニケーション重視の授業観を考察してきた。外国語教育は異文化理解能力の育成と密接に関連づけられ，語学力のみにとどまらない多面的な能力の育成が想定されている。ところで対話重視の授業では多くの困難が予想される。ベネッセ教育総合研究所（2014）の調査では，依然として英文の和訳や語彙の記憶といった伝統的な授業形態に傾いている実態が示されている。[8)]「英語ができる」ことは「長文読解力が高い，文法ができる」ことと認識している生徒

は多い。また，授業の理解度が半分以下というのが，中学では約30％であるのに対し，高校では約45％にも及ぶ。学習上の躓きとして最も高い順からあげると，「文法が難しい」ことであり，「書くこと」「話すこと」の難しさがその後に続く（これは生徒の側からの回答である）。英文法や書くことへの苦手意識が多いことは，2009年の中学生を対象とした調査結果からほとんど変わっていなかった。2015年の調査では，教員が授業で英語を半分以上使っている割合は，中学校では6割，高校では5割弱という結果が出ている。「聞くこと」「読むこと」，文法学習が中心になっていて「話す」「書く」の活動が少ないという。おしなべて，実際に英語を使うことを前提とした学習観が浸透しているとは言い難い。ごく限られた見聞であるが，筆者が2017年度担当授業の開始時点で独自に行った学生アンケートを見る限りでも，学習指導要領が謳う発信重視の学習方法への質的な転換というのは，ほとんどなされていないのが現状である。その理由として考えられるのは，⑴目標言語を使用する前のインプットの段階で多くの時間が割かれていること，⑵入学試験に対応するために言語形式の暗記中心の学習にならざるをえないこと，である。

従来型の指導では，学習者個人の中で学ぶ意欲が起き，教師の役割はいつか必要となる場合に備えて知識を蓄えさせ，そのつど学習成果の顕在化を促すというものであった。対話重視の授業観はこの流れを逆転させるものである。新しい学力観では，まず生徒が豊富な情報交換を行い，目標言語を使用した協働活動を通じて各々が知識を獲得していく。それが「分かる」喜びや実感に繋がって次の学びへの意欲が生まれるというものである。現状，目標言語の十全な理解があってこそ効果的な発信が可能になるという課題，言い換えれば，質のよいインプットをどのように行うかという昔からの課題が立ちはだかっているのではあるまいか。[9)]

学習理論においても，指導者側からの外的要因だけではなく，学習者内部の要因に焦点をあて，これらを様々な環境要因との関わりで習得のメカニズムを捉えようとする研究が盛んに行われてきた。英語教育の現場は言語習得のプロセスそのものの解明に焦点を置く第二言語習得理論の知見に大きな示唆を受けてきた。この研究は直接実用的な教授法を主眼とするものではないが，当然のことながら，現場の指導実践はこの分野の様々な研究の流れとも連動している。Krashen（1982，1985）が提唱したように，言語習得において良質なインプットを大量に行うことが重要なのは論を俟たない。インプット自体が言語習得に十分条件ではないことが主張されたのは，イマージョンプログラムを受けた子どもたちが大量のインプットを受けたにもかかわらず，文法理解が不十分だったという調査報告がなされた時である。そしてSwain（1985）らによって，理解可能なインプットとともに学習者自身によるアウトプットが第二言語習得に重要な役割を果たすことが提唱された。また言語学習における「気づき」（noticing）の重要性を説いたSchmidt（1990）は，コミュニケーション活動を通して意味と機能を一体化した指導が必要であると主張した。90年以降は，言語形式の分析が先にありきとするのではなく，他者との活動を通して自らの意見を形成し，当面の課題に取り組む中で言語規則に意識を向けさせる，いわゆるフォーカス・オン・フォーム（focus on form）が盛んに実践されるようになった。近年，英語そのものを目的とするというよりも，課題解決型の思考に重点を置きながら，学習内容を「英語で」学ぶという授業観へ次第に変質してきている。村野井（2006）は，「日本の英語教育で築き上げられてきた指導技術は，内容中心第二言語教育およびフォーカス・オン・フォームの枠組みの中で使われた場合，英語習得を効果的に促すことができる」と述べている。その言のとおり，現在では内容ベースの指導の中に時機をとらえた明示的かつ意図的な指導を組み込んでいく手法が，英語教授の主流であろう。

そして新しい学力観に照らせば，意味や内容を重視する言語活動を豊富に行い，ことばの規則性に対する「気づき」を促しながら習得を図ることが期待される。インプットとアウトプットを一体化した活動（タスク）の中で学習者自身が問題点を認識し，他者と共同で克服するプロセスを経て習得に繋げていくのが理想である。試行錯誤を繰り返し目標言語を使いながら，学習者が協調して覚えていくという学習スタイルである。従来の形式の暗記中心から実生活を反映した意味中心の実践的側面に指導の重点を置いた結果，学習効果や動機付けを高めることに成功している事例も報告されている。このような動きは，静的な記号操作としての文法学習から脱却しつつあるという意味で，大きな進歩であると言えよう。

他方で，形式の習熟に苦労している学習者がかなり多くいるという側面もある。ほんの一端にすぎないが，前述のベネッセの調査はそれを表している。本来，コミュニカティブな英語力の育成には，「本文の読み込み→発表・議論→コメント・フィードバック」の流れが，複合的な視点から物事に対する思考を深め，内容のある事柄を英語で表現する能力に繋がっていく。これは理想としてはよいように思える。だがこの活動がうまくいかなかった場合，一定の時間が経過した後で何が身に付いたか生徒自身が明確に分からないという事態が起こりかねない。現場の教師の立場からすれば，活動あって学習なしというのは最も避けたい事態である。それなら，一つ一つの言語形式の理解に拘った従来型の指導法が結果として生産的であるということもありうる。ところが，例えば，単語テストや文法テストを適宜行い，学習成果を数値化するという従来のやり方は，公平さや確実性という意味ではやりやすい反面，主体的な態度を育むという新しい学力概念にはおよそなじまないものであろう。短期記憶に依拠する従来型の学習および指導方法は，学んだことはいずれ忘れ去られ，結局役に立たないという非難がこれまで十年一日のごとく繰り返されてきた。その一方で，言語活動中心の暗示的な「気づき」を促す帰納的学習指導においても，学習内容の実質が必ずしも保証されないという点で同様の危険性を孕んでいる。発信に

繋がる質のよいインプットを内在化へと繋げるプロセスは，記憶の量だけでなく理解の深さにも大きく関わる。それには十分な時間的ゆとりがなければならないし，制約の多い教室環境の指導だけでこれを達成するのは非現実的である。

5　中間言語の複雑さと多様性

発信重視の活動をスムーズに行うには，使う言葉に有意性がありなお且つ形式の正確さにとらわれない自由な表現が許容されなければならない。この点において，即時の理解を求める明示的指導は両刃の剣となりうる。知識の一時的記憶から内在化へ昇華するには，インプットの過程で，脳内で構築した知識を整理する時間的余裕が必要である。また，正確さにとらわれない，アクティブな姿勢を求める学習形態そのものが学習の質を保証するわけではない。学習者が直面する課題は学習者の数だけ存在するといっても過言ではないほど千差万別である。ここでごく官見的な観察にすぎないが，筆者が授業で受け持つ学生が書く英文の生成プロセスに目を向けてみる。

Electric library is more common in America than in Japan. *What do you think of if I say this is true?

文法学習を多く行ってきた学生が書いた英文である。５文型や品詞を一通り理解していて，難解な英文を分析的に読むことを苦にしない学生である。後半の文について本人に質問しながらこの文の生成された経緯を追ってみた。すると文意は，「これが本当だと言えば，あなたはどう思いますか」であり，if以下は“think of”の目的語（名詞節）として繋げたという回答である。通常副詞節を導くifやbecauseが，“I wonder if…”，“That is because…” のように名詞節を導く接続詞として使われる場合があることもこの学生は知識として理解している。この文はこうした知識の土台の上で生成された英文である。ここでさらに質問をしてみる。「これは読み手に意見を求めたものか，それとも前文の情報を読み手と共有したかっただけなのか」。質問を分かりやすく言い換えると，“What would you think if this were true? ”，あるいは単純に“Do you know that?”のような表現ではいけないのかということだが，この学生は読み手の疑問を代弁する形で“Is this true?”とするだけでよかったかもしれないと答えている。

先述の“of if節”の文法解釈上の誤りは，規則の適用範囲を超えて形式を当てはめようとする，いわゆる過剰一般化（overgeneralization）の一種と考えられる。（後半の文は疑問代名詞“what”が目的語と考えれば正しい文であるが，“of”を使わないのが普通であろう）。長く文法中心で学習している学習者には，特定の規則に対する敏感期とでもいうような時期があり，冗漫な文を産出することがある。自分の知識を意識化して説明できる反面，統制面での課題を抱えていることが多い。見方を変えれば，こうした学習者は明示的指導によって，既有知識と生成した文を比較分析し，さらに聞き手からのフィードバックから「仮説検証」（hypothesis testing）を行い，英語表現に必要な操作性や簡潔性を身につけていく。これは言語発達上の建設的な誤りとして前向きに捉えられる。次のような文はどうであろうか。

How have you been? *I talk to you is since at a junior high school.

これは会話学習中心で文法にそれほど力を入れてこなかった学生が書いた文である。後半の文で言いたかったことは，“I haven’t talked to you since we were at junior high school.”（「君と話すのは中学時代以来だ」）である。主語の位置にそのまま完全文を置く誤りは，母語干渉による負の転移（negative transfer）と言えなくもないが，日本語の感覚をそのまま持ち込んでいるため，具体的なレベルでの形式習熟が求められる。この学習者に必要なのは自らの言語使用をモニターする明示的な知識としての文法である。闇雲な暗記に頼り，分析的な作業を意識して行おうとしない（あるいはできない）のも，このタイプの特徴である。母語感覚のみに頼る学習者にとって，学習年数をそれなりに重ねていても，ある時点で目標言語の強制的なインプットが与えられなければ，今後も有意性のある文を生成できないかもしれない（前半の文は暗記したものをそのまま使用したものと思われる。因みに後半の文について複数のネイティブスピーカーに解釈を求めたところ，“I have been talking to you since ~”あるいは“We have known each other since ~”などの意味で解釈した）。この場合，即時の指導内容が学習者の理解の容量を大きく超えてしまうものであれば，学習者が自信を失ってしまうことになりかねない。

ノンインターフェイス理論の体現者の一人Krashen（1982，1985）は，無意識に身につけた言語知識のみが実践的運用に繋がると主張する。これは，意識して身につけた学習英文法は実践面で役にたたないとする極端な理論である。確かに「気づき」は無意識の学習プロセスを経て突然起きることもあるし，意識化できなくても統語構造に対する直感的感覚が育っていることも重要な学習プロセスであるのはまちがいない。留学経験者であれば経験則からこのことは理解している。EFL環境においても，教室の外で英語に接する機会を多く持っていれば，教室内で学習成果が顕在化していないからといって学習が進んでいないと断ずることはできないと言える。だが，「これはおそらく正しい文ではない」とか，「正しくないかもしれないがこの表現なら伝わるかも」といった感覚による思考は，明示的指導を前提とする従来の指導現場では「理解していない」と断じられてしまうだろう。これまで第二言語習得理論が明らかにしてきたように，誤用表現や，一見意味をなさない表現上の誤りの中にも学習者なりの意図が存在する。それにしても英文の生成プロセスは非常に複雑であり，自分が作った英文について本人も説明できないことが多々ある。指導や学習効果が顕在化しなければ，指導者と学習者双方

にとって大きな不安やストレスを抱えることとなる。

アウトプットの必要条件であり，且つその後の学習を促進する「気づき」が「理解」へと昇華するプロセスは，学習者には自覚されにくい。また指導者にとってもペーパーテストだけの結果は努力の形跡は認められても，真正な学習成果として単純に鵜呑みにすることはできない。さらに言えば,「ことばを使うこと」が双方にとって（生徒にとってのことばの学び，教師にとっての適正な評価），理解の欠如を覆い隠すフィルターにすらなりうるとは言えないであろうか。いずれ，インタラクションを通じた中間言語のやりとりで，どのように学習効率をあげていくか。「態度」の評価も含めて発信型の授業ではなおさらこのような難事業に取り組んでいかなければならない。今後指導者は，これまで以上に学習者の多様性を尊重した指導が求められる。個々の学習状況の的確な把握，そして情意的側面を考慮した適度な働きかけがより必要となる。指導者と学習者が方略面での認識を共有していなければ，その後の学習の大きな推進力とはならないであろう。

6　学習環境と学習者のタイプ

学習者の多様性を把握するには指導者側の見方だけでは限界がある。学習者自身が自らの認知的傾向を知っておくことは，情意的側面において非常に有効であるように思われる。ここでは，和泉（2016）が紹介する分析と統合の２次元モデルを参考に，学習環境と学習者タイプとの関わりを踏まえ,今後向き合うべき課題について考えてみたい（図１）。このモデルは言語使用の正確さと流暢さの関係を示している（以下,『分析と統制の２次元モデルの概観』の一部を要約させていただく。これは和泉が指導方法を考える前段階として提示したものであり，英語学習者の現状の発達過程を統計として纏めたものではない）。

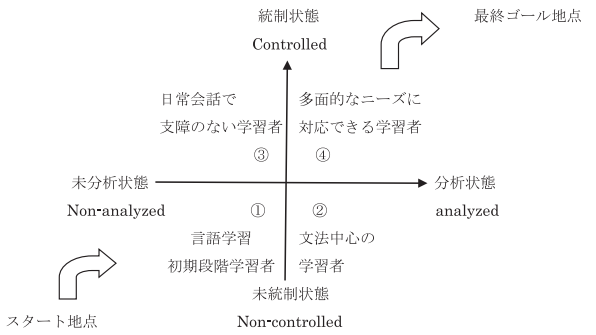

図１　分析と統制の２次元モデル（和泉2016）

①の学習初心者が本来的に理想とする総合的な「英語力」は，分析力（言葉の規則内部構造が理解できる力）と統制力（言葉を即座に活用できる力）の両方を兼ね備えた，①→④へ向かう事態である。しかし，現実的には①→④へ直線的に進むわけではなく，①→②または①→③の次元のどちらかに偏るのが普通である。和文英訳や英文和訳など言語形式重視の英文法を中心に学んだ学習者は，①→②の次元に進んでいく。しかし，このタイプは統制力が未発達なことから即興性を要する実践面で支障がでてしまう。一方，①→③の次元へ向かう学習者は，限られた表現を駆使して日常会話をこなすことができるが，難易度の高い複雑な内容についての読み書きが困難になる。

言語の発達プロセスは，学習環境や生活状況といった外的要因（学習環境や教授方法）に加え,学習者内部の要因（性格，動機付け，個人差など）が複雑かつダイナミックに絡みあっている。この二元的図式で詳細な実相を判断することはできないが，新旧の学力観における学習環境とその影響に関するおおよその類型を示してくれている。

受容一辺倒の伝統的な教育では，表面上は①→②のプロセスを志向しているように見える。すぐには使えなくても，高校や大学受験などが道具的動機を暗黙のうちに支えており，学校での定期試験や模擬試験の結果が当座の英語力と関連付けられる傾向にあった（少なくとも学習者の中では目に見える試験結果と自分の英語力を一体ととらえていた）。そのため，使えない英語の象徴的存在として「受験英語」と一括りにする表現が流布することになったが，本来的には，いずれ成果が開花しうる期待のもと，潜在的能力を養いながら④のエリアに向かう土台作りを志向したものである。これは明示的知識によって後の効果的な学習が可能になり，いずれコミュニケーションの実践に役立てられるという考え方（インターフェイス理論）を前提としている。この学習環境では，十分な語彙力や文法力がありながら統制面でうまくいかず，不幸にも英語への苦手意識をもつことになった学習者が少なからずいたものと思われる。一方，発信を主眼とするコミュニケーション重視の新しい学力観は，４技能を有効にインタラクトさせて教室をライブな言語活動の環境に整え，学習者主体の体験型，協働的な活動を通して④のエリアを目指すものである。「積極的な態度」を重んじるこの授業形態では，一見学習成果が顕在化しているようでありながら，その実，分析力が未発達なために限られた範囲の表現しかできない学習者が出てくることが予想される。

異なるタイプの不足した部分を補償する意味でも，今後共同的な学びがより推進されていくことになるだろう。上述の「分析型」と「統合型」の学習環境の違いは，学習者の認知スタイルの違いにも何らかの相関があるものと思われる。Brown（2000）は「場独立性」（field independence）の強い学習者と「場依存性」（field dependence）の強い学習者の分析を行っている。前者は部分を綿密に分析する能力に優れ，特定の項目を集中的に扱うテストで力を発揮しやすい。独立心が強く，即時の明示的な指導で学習効果をあげられるタイプであろう。一方，後者は細かい項目を扱ったペーパーテストでは力を出せない場合もありうるが，周囲への依存度が高い反面，対人関係を築くのが得意である。他者と関わる自然な環境の中で学んでいけるタイプであろう。もちろん，すべての学習者がいずれのタイプに属するということではない。これには

生得的な要因も複雑に絡んでいるだろうし，教室環境，学習到達度あるいは情意的要因などによっても両極間を不安定に行き来することになる。

結　　論

前述の和泉の２次元モデルに基づけば，新旧の学力観の違いによって，目指すべきものが大きく変わるというのは実態に即した見方ではない。問題はこれらの学習環境を対立したものと捉えてどちらが望ましいかを議論することではなく，両輪の総合的な学力の適材適所を考えていくことであろう。この意味で，特定の指導方法のみに傾倒することや，普遍的な枠組みでの目標設定が曖昧なまま，特定の指導法の是非を論じることにもあまり意味がないと言える。

学習指導要領の内容に戻って言えば，英語で授業を行うべきか否かということもそれ自体が本質的な問題とは言えない。新学習指導要領の方針から和訳や母語使用が否定的に捉えられてきたが，かつて形式に偏重する「訳毒」と揶揄された文法訳読法も現在では少しずつその効果が見直されてきている。教材内容の抽象度が高いほど母語による指導が，ことばに対する深い思考と内容理解の助けになるだろう。外国語を理解するうえで積極的に母語を取り入れる授業観を肯定的に捉える研究者もいる（Cook 2001）。こうした動きに注目して，伊東（2016）は和訳をコミュニケーションの一技能として再評価し，具体的なリーディング指導を提案している。思索が多方面にわたるため，ここでは詳しく検証することはできないが，伊東が提示する方法論に基づいて，平成以降コミュニケーション重視の授業の影で冷遇されてきた和訳学習の意義をまとめておきたい。

⑴　英文和訳を内容重視のフォーカス・オン・フォームの一形態として見直し，それをインタラクティブな指導実践に応用していくこと。
⑵　欧州が推奨する複言語主義の観点から，外国語学習における母語介入の適材適所を考え，視野の広いトータルなことばの教育を実現していくこと。

“Post-method Era”と呼ばれる現在，教師は知識伝授者というよりも主体的な学びを補助する助言者（advisor, accommodator）としての役割がますます大きくなっている。これは指導の限界ではなく，現場の実情にあわせて対話ベースの多様な試みが許容されることを意味する。異種混淆を容認するグローバル社会は“glocal”を異称とする。今後の英語教育では４技能統合という学習スキルに加えて，学習活動に直接関わらない方略，即ち間接的ストラテジー（indirect strategy）の重要性がこれまでより増してくることになるだろう。言語習得における「意識」や「気づき」は，実態が曖昧であるがゆえに様々なレベルで論じられてきた。これらの概念は，学習を管理する面においてまた教育的観点からも，最も根源的な対話の営為となるはずである。具体的にはOxford（1990）が提唱する学習ストラテジーを構成する要素であるが，この理論に基づいた試みは特に新しいものではなく，一部の高校や大学で既に独自のスタイルで実践されている。指導者が特定できない習得プロセスがある点を考慮し，学習者が自らの学習を管理する自律学習に向けた方略をより具体化していくことが必要かもしれない。それは指導者の“skill”と，“potential communicator”としての学習者の自己診断が相補完的に機能するという意味での方略である。

＜註＞

1）本文中，学校教育の現場に限定して指導・学習に関わる者をそれぞれ「教師」,「生徒」とし，学校教育を含むすべての場面で英語の指導･学習に関わる者を「指導者」,「学習者」と表記することにする。また本稿は，学習指導要領の文言に寄り添って論考していくが，そこで示されている個別の学習内容や指導方法そのもの是非や，目標設定に関する普遍的な枠組みでの正当性や有効性については関心の埒外にある。
2）学習指導要領の策定プロセスやその背景にある言語政策については，『危機に立つ日本の英語教育』（2009）の論者たちに代表されるように批判的に論じられてきた。「授業は英語で」の部分は特に大きな反響を呼んだ議題の一つである。私見では，施策としてオールイングリッシュを強制することは批判の余地はあると思うが，実情にあわせて英語使用中心の様々な試みがなされることは大変よいことであると考えている。なお，2010年公示の学習指導要領解説では，「状況に応じて英語で行う」とし，オールイングリッシュによる指導を完全には義務化しない方針に変えられている。
3）学校教育法第三十条第二項では，「生涯にわたり学習する基盤が培われるよう，基礎的な知識及び技能を習得させるとともに，これらを活用して課題を解決するために必要な思考力，判断力，表現力その他の能力をはぐくみ，主体的に学習に取り組む態度を養うことに，特に意を用いなければならない」と規定されている。
4）鈴木氏はそれまでの英語教育最大の問題点として使用目的が不明確である点を指摘し，様々な異種より成る国際補助語としての英語学習を教育の目的とすべきであると主張していた。
5）2020年度から始まる大学入試センターに代わる「大学入学共通テスト」（仮称）の実施方針案が2017年５月16日に公表された。英語は民間の試験を想定し，「話す」「書く」も含めた４技能を測る方式に大きく転換する。試験の実施・評価方法をはじめ，地域・学校ごとの公平性の確保など多くの課題が指摘されている。また，入試の外部移行によってこれまで以上に成果主義に傾いていく懸念も拭えない。
6）2013年度施行の高校学習指導要領改訂案が発表された時，その作成に携わった松本茂氏は，教師による解説や訳読などで時間が費やされることを問題視し，授業を生徒中心のコミュニケーション活動としてできるだけ英語を使うことを推奨した。『危機に立つ日本の英語教育』の著者である大津由紀夫氏は，母語を基盤とした言語教育の重要性を説く。英語の仕組みを身につけなければ英語が使えるようにはならないと述べ，英語のみによる指導には反対の立場をとっている。この件とは関係ないが，鳥飼（2011）は，コミュニケーションとは何かを具体的に議論されないまま英語教育改革が行われたため，単純に英会話と解釈されてしまったことを，英語教育の現場が混乱した原因として指摘している。

７）文部科学省がOECD加盟国によるPISAの学力到達度調査を念頭においているのは明らかである。早くからアクティブラーニングが授業の中核となっている欧米諸国に比べ，日本を含めて旧教育が依然として行われている東アジアの国・地域の成績が常に上位を占めている点は興味深い。

８）筆者は文法訳読式教授法に代表される伝統的な指導形態に異を唱えているわけではない。従来の学習方法が主体性を欠き課題解決型の学習（指導も含めて）をしてこなかったというのは明らかに事実に反する。明治時代から長い歴史で培われてきた教授法も，英語習得に成功した例として引き合いに出される歴史上の偉人達も，その時代にあった課題解決型の主体的な学びをまさに体現している。本来，課題解決型の学習という際，学ぶ側に対して明確な目的があり適切な学習を行っているか，学習内容にどれだけ価値を見出しているのかが問われるべきであろう。

９）多くの論者が指摘するように，日本のようなEFL環境では規則の概念的理解から実際の使用に繋げていくには教室内での学習では圧倒的に時間が不足している。大勝(2012)は，英語との言語距離が近い欧州諸国と比較しても，日本における中学校・高等学校での英語の総授業時間数が少ないことに触れ，英語母語話者からみた外国語の難易度に基づき，習得に必要な時間を試算している。それによれば，日本の生徒にとってドイツ語を母語とする生徒が到達する英語レベルに追いつくには約４倍もの学習時間が必要だという。

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